THE APPLICATION OF CODE CONVERSION TECHNIQUES TO DIGITAL AUDIO SYSTEMS

by

Stephen A. Wilcox B.Sc., A.M.I.E.E.

A thesis submitted to the University of Keele
for the Degree of Doctor of Philosophy

May, 1982

Signal Processing Group,
Department of Physics,
University of Keele,
Staffordshire,
England.

ORIGINAL COPY TIGHTLY BOUND

"That is innovation

That is evolution

That is civilisation"

The words of Akio Morita, co-founder of the Sony Corporation of Japan.

He first used them to encourage friends who, in the 1950's, doubted the value of buying two loudspeakers for the then new-fangled stereo system. On April 15th 1981 he repeated these words again, this time to stimulate those who perhaps view the advent of the domestic digital audio system with similar circumspection.

ABSTRACT

The recent development of low cost digital storage has made digital audio systems attractive. However its popularity depends on the development of accurate low cost digital to analogue (D/A) converters. Existing converters require the fabrication of precision analogue components which prohibit their mass production. An alternative strategy is investigated which involves code converting the digital P.C.M. into a different digital code which can be simply decoded. This type of D/A converter removes the need for precision analogue hardware at the expense of increased digital complexity and is therefore more suited to mass production.

Code conversion to delta sigma modulation is investigated and found to be unsuitable for high quality audio at practical clock frequencies. Methods of improving the performance of the basic d.s.m. by shifting the encoding noise out of the message band by changing the P.D.F. of the input signal are investigated and shown to be unacceptable for a linear system.

An error feed-forward converter is described which uses a second d.s.m. to encode the residual error produced by the main d.s.m., thus achieving a useful reduction in quantization noise. The order of the feedback filter is increased in the proposed second order system. This is shown to give 14-bit P.C.M. accuracy at a 4 MHz clock frequency.

An additional advantage of using these code converters is illustrated when they are used in conjunction with a class D power amplifier. This arrangement eliminates the need for any analogue processing.

ACKNOWLEDGEMENTS

I would like to express my grateful thanks and appreciation to:

Professor W. Fuller for the provision of research laboratory facilities.

The Science and Engineering Research Council for providing the finance necessary to undertake this research.

Dr. M.J. Carey for the initial ideas and encouragement.

Mr. G.D. Tattersall for his excellent supervision and encouragement during the writing of this thesis.

Mr. G. Dudley and the staff in the workshops for their help in constructing the equipment.

Mr. M. Daniels for the preparation of the photographs.

Mrs. E. Durrant for her assistance with administrative work.

Miss H. Martin and Mrs. K. Merifield for their excellent work in correcting and especially typing this thesis.

The many members of the Physics Department, especially my research colleagues Colm, Ambi, Aladdin and Kamran, who have helped to make the last three years enjoyable and stimulating.

Miss Janet Turner for her help with the preparation of the diagrams and the photocopying of this thesis.

CONTENTS

CHAPTER 3 (continued)

CHAPTER 1

INTRODUCTION

1.1 An Historical Perspective

It is just over one hundred years since Edison took out his patent in the U.S.A. which gave birth to the gramophone industry. Since that day, 24th December 1877, technology has advanced a long way. However, it is only in the last decade that the inherent robustness of digital techniques has begun to find a place in the recording industry.

1.1.1 The Development of the Hi-Fi Industry

Edison's original idea was to scribe analogue signals onto the side of a slowly revolving wax cylinder; replay was accomplished simply by causing a diaphragm to follow the groove. This method suited the available technology since it did not require any active components, although the quality of reproduction was very poor by today's standards.

The aforementioned wax cylinder, originally nothing more than a novelty, unwittingly founded the gramophone industry which, over the last century, has continued to improve the quality and range of music available. These improvements are the outcome of a battle between any recording system's two main components:-

i) The storage medium

ii) The reproduction system

Wax cylinders were soon replaced by the Shellac 78 discs, which could be mass-produced. Despite having limitations in bandwidth and playing-time, it remained the standard for many years. Advances in pick-up design, amplifiers and loudspeakers eventually caused the 78 disc to become the weak

link in the quest for high fidelity, resulting in the introduction of the E.P. and L.P. records of today. The latter revolve at slower speeds, giving longer playing times; better quality materials also made it possible to fit grooves closer together.

The modern vinyl L.P. disc is far less fragile than the wax cylinder or Shellac disc, and is able to give hitherto undreamed of Hi-Fi stereo reproduction. It is also a superb gatherer of dust; each speck will damage the vinyl structure permanently. A modern cartridge tracking at less than one gramme causes slight damage to the groove pattern.

The maximum deviation of a record groove is 25 μm and ideally to achieve full dynamic range, a cartridge must be able to track the individual molecules of vinyl. Given this situation it seems likely that in the near future, if not already, the development of the analogue record will reach stagnation point, making it once again the limiting factor in the performance of the recording system.

One solution was thought to lie in the use of magnetic tape as an alternative storage medium. Although tape cannot be scratched and interference due to external influences is much less common than the effect of dust on records, it does produce tape-hiss, which is an intrinsic feature of the material itself. Tape, especially the narrow cassette variety, has non-linear magnetic and audio characteristics, hence high-fidelity recording is a triumph over adversity. Recent developments in noise reduction systems (Ref. 1.1) have helped to make tape, in the form of the compact cassette, more popular today than ever before. The introduction of metal tape has shown that further improvement of tape materials can still take place. The fact remains that tape is unable to give the quality of a direct-cut disc at a competitive price. It is also unlikely that analogue tape systems will improve dramatically during the next decade.

In summary, analogue recording methods inherently suffer from noise and non-linearity, are easily damaged and no method is available for correcting errors or even detecting anything except simple scratches. It is to effect a solution to these problems that an interest in digital techniques and their possible exploitation in music recording has begun.

1.1.2 The Introduction of Digital Techniques

The need for digital audio is more apparent now that the limitation in current analogue systems has been considered.

As a digital signal is transmitted it will accumulate noise and undergo distortion just like analogue signal, however, digital signals can be regenerated into a perfect copy of the original. This is possible because a receiver can work with low signal to noise ratios, only having to decide whether the input signal is a logic one or not. A large amount of redundancy can be added to the digital signal in the form of error correcting codes, which can correct errors produced by bursts of noise, drop-out, or receiver errors. This is only possible because the range of digital signals is finite. Existing transmission and storage systems may be up-graded by employing suitable digital codes to produce systems with extremely low error rates which produce no perceivable degradation in performance.

Using digital techniques, the weakness of the storage medium has been removed at the expense of bandwidth and the quantity of storage required. The performance of a digital system depends on the type of code adopted, which in turn determines the number of bits and sample rate used. A typical digital system encoding a 15 kHz quality signal would require a 512 kHz bandwidth. Although large, this bandwidth requirement has become less of a problem with the introduction of mass storage systems and experience gained in the computer industry.

1.1.3 Digital Systems Currently Available

The advent of digital transmission systems for high-fidelity audio systems has resulted in a number of similar yet incompatible systems.

One of the first systems to come into operation was developed by the B.B.C.. The PCM link between Broadcasting House and the Wrotham transmitter (Ref. 1.2) has been in use since September 14th 1972, and has subsequently been extended to form a distribution network for all their high quality radio transmitters. The sampling frequency is 32 kHz, using a 13 bit linear PCM encoding. A sampling rate of 32 kHz has been accepted as a European standard for digital transmission systems.

Many recording studios are now using digital systems, either for processing or for producing digital master tapes. The first records to benefit were those of the Nippon Columbia Company which produced a conventional analogue record from a digital master tape. The recorder used 13 bit linear PCM at a sample rate of 47.25 kHz. Similar systems have now been produced by most recording companies.

Sony have produced an additional add-on unit (Ref. 1.3) for their range of video-recorders to enable high-fidelity audio to be recorded. This system uses a sample rate of approximately 44 kHz and claims an accuracy of 16 PCM bits. Not all systems use linear PCM; some manufacturers have decided to use companded systems (Ref. 1.4), but only because suitable linear converters have not been available. Current digital-audio techniques employ a variety of sampling frequencies within the range 32-50 kHz, and many different encoding formats. Recording systems which adapt video tape-recorders require a sample frequency which must be a sub-multiple of common colour television frame and line frequencies; these appear to be converging on 44.0559 kHz. This is considered too low for professional use, which requires rates in excess of 50 kHz. The actual number of PCM bits and the type of code used depends on the individual manufacturer, with 16 bits considered satisfactory for professional use.

1.1.4 The Digital Disc

Up-dating the record disc for the use of digital codes has necessitated considerable development to accommodate the increase in bandwidth. The compact disc is now recognised as the new standard (Ref. 1.5).

Unlike a conventional grooved record, the compact disc is read optically. A beam of light from a miniature aluminium-gallium-arsenide diode laser is focused on the spinning disc. Tiny pits in the disc modulate the intensity of the reflected beam, then a photodiode converts it into a varying signal.

The use of this optical play-back system eliminates record wear. The effects of noise, dust, scratches and distortion in the pick-up system are eliminated by the error-correcting codes. Re-timing the recovered information using a buffer memory eliminates wow and flutter. Specifications of the compact disc are shown below and compared with a high quality analogue record system.

	Analogue Record System	Digital Compact Disc
Signal to Noise	70 dB	95 dB
Dynamic Range	35-40 dB	95 dB
Harmonic Distortion	0.2%	0.03%
Wow/Flutter		Equal to Xtal Oscillator
Modulation Type	Moulded grooved PVC	16 bit linear 2's Complement PCM

Other disc systems have been proposed, (Ref. 1.5) some using a piezo-electric pick-up which varies its capacitance according to the information

stored on the disc. However, all have been superseded by the compact disc.

Acceptance of digital audio systems will depend on their cost to the consumer. The cost of producing the compact disc is largely determined by the cost of the scanning laser and associated digital to analogue converter. All the major semiconductor manufacturers are trying to reduce the cost of these digital to analogue converters whilst retaining the required accuracy. Different types of digital codes are discussed in the remainder of this chapter; the main report describes construction and performance of alternative low cost converters.

1.2 Requirements of a Hi-Fi System

If an abstract high-quality wide-band audio signal is considered, two main characterizing quantities of amplitude and frequency can be considered. The signal consists of a complex, rapidly-fluctuating voltage within an infinite range of levels.

1.2.1 Spectrum

The work of Fourier (Ref. 1.6) showed that these complex waves can be considered as the sum of a set of sine waves having different values of amplitude and phase. For example if middle A is sounded on a piano, a fundamental frequency of 440 Hz is produced, but it is the set of odd and even harmonics extending well beyond the human range of hearing which give it the characteristic piano sound; without them it would sound like any other middle A. Hence for absolute fidelity the unique harmonic fingerprint of the signal must be preserved.

1.2.2 Dynamic Range

The dynamic range of the human auditory system has been estimated at 130 dB (Ref. 1.7) yet in practice the lower level is masked by background noise and the upper level causes physical pain. It has been suggested that

a dynamic range of 90 dB is required for the full range of live music to be appreciated, and for a linear system a peak signal to noise of greater than 90 dB would be required.

1.2.3 Practical Analogue Limitations

Whenever a wide-band audio signal is fed directly onto tape or disc all the mixing, amplification and modulation take place in analogue form. The set of processes involved in bringing a recorded performance into the home is very complex, with many separate processes each introducing its own form of degradation.

It is current practice to record each performer on a separate track of a multi-track recorder, giving the producer a high degree of flexibility. However, this results in a flat sound since live performances contain considerable reverberation and spectral biasing which must be added artificially. Each track then undergoes more signal processing and the final sub-master tape is a complex blend of the original tracks.

During the mix-down, it is necessary to take into account the limitation of the storage medium, (either tape or disc,) and apply compression to limit the dynamic range. This is because professional master tape recorders, although built to a high standard, can only produce signal to noise ratio of about 70 dB. The noise mechanism is not static, but is modified by the signal resulting in programme-modulated noise. This kind of noise is very perceptible when the signal is around 1 kHz, and under this condition the signal to noise ratio can fall to less than 40 dB.

The ultimate limiting factor in analogue storage is the record disc itself. Analogue records have a maximum signal to noise ratio of 65-75 dB (Ref. 1.8) with useable dynamic ranges of only 62-64 dB. Under ideal conditions, distortion in a phonograph cartridge is rarely less than 0.1% and typically 1-3%.

The total noise and harmonic distortion heard by the listener is

accumulative, each stage contributing some degradation. Attempts are made throughout the whole chain to reduce these effects to a minimum (Ref. 1.9); nevertheless, there is a definite limit to the amount of signal processing which can be employed before the final product becomes unacceptable. Records made directly in real time, without using master tapes, display superior performance and show greater depth and crispness. These 'direct cut discs' are the best available using analogue processing.

1.3 Digital Coders

When using digital signal processing, the level of distortion and dynamic range are solely a function of the type of digital code used and the associated analogue to digital and digital-analogue converters. Once information is converted into digital-form processing, transmission and storage can easily be effected with no loss of information or quality. In assessing the performance of digital systems, it is necessary to consider the available dynamic range and level of quantization error (Ref. 1.10). Of the many digital codes available, linear PCM offers a predictable no-compromise solution, and is frequently used as a reference.

1.3.1 Ladder Network D/A Converters

Most integrated D/A converters use an R-2R ladder network to generate binary weighted currents. These currents are switched by individual bit-switches and summed in an operational amplifier to produce the required output voltage. This type of converter is shown in Figure 1.1. There are two main design problems in this system.

The first problem concerns matching the resistors in the ladder network to give the required accuracy; current fabrication techniques (Ref. 1.11) give only 10-bit accuracy. To obtain 12 and 14 bit accuracy it is necessary to use individual laser-trimmed thick film resistors, or

make use of specialised techniques such as "dynamic element matching" (Ref. 1.12).

The second problem occurs when changing the state of the digital switches. If all the switches do not change simultaneously, a glitch will be produced on the output as an incorrect digital code is momentarily presented to the ladder network. To remove these glitches a sample and hold circuit must be placed on the output of the D/A converter.

When high accuracy ladder D/A converters are mass produced these additional techniques and the need for a de-glitcher circuit increase the overall unit cost.

If a system which did not require any individual trimming or additional output circuitry could be produced on a single L.S.I. chip, the cost of high accuracy D/A converters would be significantly reduced.

1.3.2 Linear PCM

Consider the general digital audio system shown in Figure 1.2, which makes use of linear PCM. The incoming analogue signal is first low-pass filtered by a sharp cut-off filter to remove any incoming frequencies above $F_s/_2$. This band-limited signal is then sampled by the sampling circuits and held to allow analogue to digital conversion to take place. The resulting output is a series of digital words, each corresponding to a sampled input level. Once into digital form the signals can be processed, transmitted or stored as required. To return it to analogue form each digital word is converted into a discrete analogue level by the digital to analogue converter and then the output low-pass filter smoothes these discrete samples into a continuous signal. Given perfect conversion processes, the main source of error results from quantizing the input signal, which leads to a theoretical maximum error of half a quantization interval. This is related to the number of quantization levels, and hence to the number of bits in each digital word, as shown below:-

N = Number of levels
n = Number of bits

$$N = 2^n \qquad 1.1$$

If the input signal is at a high level with wide bandwidth, then the quantization error produced has a rectangular probability function. As a result, the quantization error has similar properties to those of additive white noise, often referred to as quantization noise. Using equation 1.2 it is possible to calculate the maximum RMS signal which n bits can accommodate:-

$$Vs\ (R.M.S.) = \frac{Q\ 2^{n-1}}{\sqrt{2}} \qquad 1.2$$

Q = size of quantization interval

To derive the power of the quantization noise it is necessary to obtain the power of each error and the probability of it occurring. This gives the expression shown below:-

$$Vn\ (R.M.S.) = \frac{Q}{\sqrt{12}} \qquad 1.3$$

By combining 1.2 and 1.3 the standard result for the maximum signal to noise of linear PCM can be obtained:-

$$SNR = \sqrt{1.5}\ 2^n$$

$$SNR\ (dB) = 6.02n + 1.76$$

The above expression shows that each bit contributed 6 dB to the obtainable SNR. In the linear system described, the useable dynamic range is approximately equal to the maximum signal to noise ratio. Differences occur because of the need to allow a margin of headroom to permit high-level high frequency signals to pass through the system without being clipped.

Consider a low-level sinusoidal signal whose peak amplitude just crosses one quantization level; the digital output will then take one of two possible levels, depending on the sign of the input signal. In effect, the outcome will be a square wave, and this non-linear operation results in

harmonic distortion as opposed to a wideband noise. If this process occurs at a high frequency, significant harmonics can be generated above half the sample frequency and these will be aliased back into the message band, resulting in the generation of new non-harmonically related frequencies. This new quantization error is neither noise nor distortion in the classic sense, and is particularly noticeable subjectively.

1.4 Types of Digital Codes and Converters

Although linear PCM offers a no-compromise encoding system, it does require large numbers of bits. There are various types of converter in service today, some using different codes similar to PCM, others using a one-bit code. This section outlines briefly some of the well-known alternatives to linear PCM, highlighting their main attractions and disadvantages. At the end of this section, a comparison is made between each system's performance, as a function of bit rate. This is considered necessary in order to explain why some systems have won favour in the commercial world.

1.4.1 Floating Point Converters

To provide the required dynamic range discussed in section 1.2.2 a linear PCM converter would require 16 bits, resulting in a high storage and processing cost. For low-level signals, the full 16 bits are required; however, when large signals pass through the system, any noise caused by a reduced number of bits would be masked by the wanted signal. Thus, any system which can reduce the number of required bits, yet still give the same perceived performance, offers considerable economic advantages.

A floating-point converter produces a digital output word which can be split into two parts:- exponent and mantissa. It is convenient to consider the exponent as representing a quantized variable-gain amplifier, preceding a conventional linear PCM converter; such an arrangement is shown

in Figure 1.3. In standard PCM, low-level signals span only a few quantization levels, producing poor signal to noise levels, since few levels are actually used. In the floating point system, the signal is amplified such that it fills all available quantization levels, the amount of amplification used being determined by the input signal level. Hence the relative quantization level changes according to the level of input signal, although the absolute level of quantization noise is constant in the mantissa. The amount of amplification used is encoded in the exponent and both exponent and mantissa are transmitted as a single digital word. A floating point system's dynamic range is always greater than the peak signal to noise. The total dynamic range of this conversion technique is the sum of the mantissa's dynamic range which is determined by the number of bits and the range of pre-scaling used, each pre-scaling level adding 6 dB to the dynamic range. If a practical system with a 3-bit exponent and a 10-bit mantissa is considered, the available dynamic range is 102 dB but the maximum SNR is only 60 dB. This relationship is shown in Figure 1.4. The system described must be able to change the pre-scaler gain instantaneously to allow for fast transients in the input signal. As a result of the gain changing, the level of noise will also change, resulting in programme modulated noise which is particularly noticeable if the amplifier gains are not accurately matched, resulting in a non-linear transfer characteristic. One solution to this problem can be found in the syllabic floating point algorithm. With this type of codec the algorithm adjusting the pre-scaler is given a fixed time constant. The syllabic algorithm decreases the gain whenever the converter would have been overloaded, but does not increase it until the signal has remained at a low level for a pre-determined period, which corresponds to a typical musical syllable.

1.4.2 Companding Systems

The floating point converter previously described can be considered

as a special case amongst the group of non-linear coders which use companding to give increased dynamic range. Generally, the spacing of the quantization levels ensures wide spacing for large signals and close spacing for small signals. Regardless of the non-linear quantization intervals, this type of system can be modelled on a linear PCM system with non-linear elements on the input and output. This arrangement is shown in Figure 1.5. There are many types of companding systems which determine the shape of the transfer curve (F(x)), and all attempt to change the quantization level spacing in such a way as to reduce the perceived level of programme-modulated noise.

The more common systems, known as A-law and μ-law use instantaneous companding in which each sample is independently coded (Ref. 1.4). However, the B.B.C. and other broadcasting companies have developed companding systems which perform "near instantaneous companding", (Ref. 1.13). In such systems, successive blocks of digital samples typically 32 samples long, are coded to an accuracy determined by the size of the largest sample in each block. A separate scale-factor word is transmitted to the decoder so that the appropriate scaling can be achieved. This type of system results in considerable reduction of programme-modulated noise, since the changes in scaling occur at a low frequency not normally perceptible. Currently the B.B.C. is reviewing its specification of digital link equipment; it is likely that the present use of 13 bit linear encoding with dither (Ref. 1.14) will be replaced by a companding system known as NICOM 3 which gives a 14 bit linear quantization with 10 transmitted bits.

1.4.3 Differential Pulse Code Modulation

It is possible to achieve a reduction in the number of transmitted bits by digitizing the difference between successively sampled analogue signals. This is possible because the dynamic range of the difference

signal is small, hence less bits are required to digitize it. This type of encoder creates a prediction for the current signal based on previously transmitted data. The diagram in Figure 1.6 shows a typical differential PCM system. At first sight this approach seems attractive, however, it is interesting to observe the effect of quantizing the difference signal on the overall noise spectrum. In a differential PCM system the sampled input signal is delayed by τ, equal to the sampling period and subtracted from itself, so producing a difference between successive samples. This difference is then digitized by the A/D converter and transmitted. The quantized signal is accumulated by the decoder to form the output; the output of the A/D converter, (Y(t)) is related to the input signal by:-

$$Y(t) = X(t) - X(t-\tau) \qquad t = n\tau \qquad 1.5$$

Equation 1.5 represents a differentiating filter with a transfer function given by:-

$$H(s) = 1 - e^{-s\tau} \qquad 1.6$$

It is now possible to model the differential PCM codec by a linear PCM codec preceded by a filter whose response is H(s). This is equivalent to pre-emphasis; similarly, the decoder provides the input with de-emphasis. It has previously been shown that PCM encoding gives a flat quantization noise spectrum, thus the output noise spectrum will be changed due to the de-emphasis filter producing an undesirable 1/f noise spectrum. It is possible to reconfigure the coder shown in Figure 1.6 to produce a flat output spectrum, as shown in Figure 1.7. The difference signal, which is encoded by the PCM encoder, is now composed of the input signal and a reconstructed output signal identical to the one produced by the decoder. Due to the feedback introduced, large errors in x(t) cannot occur at the decoder because these errors have been re-introduced into the encoding

path. It can now be shown (Ref. 1.15) that noise, (due to quantization) is filtered by the function:-

$$G(s) = e^{-s\tau} \qquad 1.7$$

The above is a phase delay and thus the noise output spectrum is flat, as in conventional PCM. Overall, there is an increase in the available dynamic range at low frequency at the expense of dynamic range at high frequencies. This may not be an advantage if the system is used to encode wide-band music.

1.4.4 Delta Modulation

There are a number of different types of converter which can be termed Delta Modulators; all produce a one-bit code, some extremely simple in construction, others very complex, but giving enhanced performance.

1.4.4.1 Linear Delta Modulation

In linear delta modulation (LDM), it is the level difference between samples which is represented as a one-bit code, (unlike linear PCM, where the absolute magnitude of each sample is transmitted), so, provided the magnitude of the previous sample is known and that sufficient samples have been taken, accurate information is transmitted.

This type of converter, shown in Figure 1.8, has the big advantage of simple hardware which does not require sample and hold circuits. Moreover, anti-aliasing filters are not needed because the sampling rate is usually very high compared to the message band.

At each clock instant, a decision is made by comparing the input signal with a locally-derived approximation signal. A small positive increment is added to the approximation signal if the initial comparison proved negative; conversely, if the comparison proved positive, a negative amount would be added. When this process is repeated at every clocking instant, the approximation signal tracks the input signal, indicating correct

encoding. The approximation signal is formed by integrating the one-bit digital output, hence a remote locally decoded signal can be obtained by the same process. This type of single bit converter produces two main types of signal error. Firstly, there is an obvious limit to the rate at which the approximation signal can be increased or decreased, i.e. when the signal is changing by more than one approximation signal increment every sample period. This effect is termed 'slope overload' and is analogous with slew-rate limiting. Secondly, at the other end of the encoding range, then the signal input is less than one increment, the encoder is now unable to decide accurately whether the signal is changing, consequently the coder produces a series of ones and zeros known as the idle channel output. The pattern is disturbed when the input signal exceeds the quantization threshold, and the error produced in this case is similar to PCM quantization error. A more detailed account of LDM is given in Appendix 1 where it is shown that:-

$$\text{Dynamic Range} = \frac{f_m}{\pi f_s} \qquad 1.8$$

$$\text{Signal to Noise} = \frac{1}{8\pi^2 k_q} \left(\frac{f_m^3}{f_s(\max) f_s^2} \right) \qquad 1.9$$

f_m = clock frequency $\qquad$ f_s = mod. frequency

k_q = constant

1.4.4.2 Linear Delta Sigma Modulation

It can be seen from equations 1.8 and 1.9 that conventional LDM has the disadvantage that the dynamic range and signal to noise ratio are inversely proportional to the signal frequency. This is an obvious disadvantage for encoding high quality music signals which have flat frequency spectra. The problem arises through the inevitable differentiation of the input signal, but it is simply overcome by inserting an integrator

at the input of an LDM encoder and preceding the decoder by a differentiator. Such a system is shown in Figure 1.9. Since the transfer function of the two integrators are identical the system can be re-configured as shown in Figure 1.10. Similarly, in the decoder, the integrator and the differentiator can be omitted. The system shown in Figure 1.10 constitutes a Linear Delta Sigma Modulator, LDSM.

Thus the chief advantage of LDSM over LDM is that the former has a flat frequency/amplitude characteristic, and overload occurs at the same level for all frequencies. This is at the expense of the quantization noise spectrum not being flat, but rising by 6 dB per octave with a corresponding rise in the low-level encoding threshold.

One important advantage of LDSM is that only one filter is required for decoding. With reference to Appendix 1, the dynamic range and signal to noise are given by:-

$$\text{Dynamic range} = \frac{f_m}{\pi f_s}$$

$$\text{Signal to noise} = \frac{3}{8\pi^2 k_q} \left(\frac{f_m}{f_s(\max)} \right)$$

1.4.4.3 Predictive Delta Modulation

There are many techniques available for improving the performance of delta modulators, including techniques to change the quantization step size (Ref. 1.16) according to an algorithm; other systems integrate the error signal (Ref. 1.17) to produce a double integration system, and various techniques are used to change the output noise spectrum to put the quantization noise out of the required message band, (Ref. 1.18). All of these, however, are only suitable for specific applications when it is possible to make accurate assumptions about the spectrum of the input signal.

1.4.5 Summary

This section has outlined the different types of digital conversion techniques available. Briefly, they are as follows:-

(a) A PCM system can be considered optimal for signals which have an equal probability of spanning the entire amplitude and frequency system.

(b) The floating point system assumes that high-level and low-level signals occur in groups.

(c) Adaptive systems assume that a signal's spectrum is dominated by low frequency energy, since the adaption algorithms are slow to respond.

(d) Differential pulse code modulationcan give a saving in transmitted bit-rates at the expense of high frequency performance.

(e) Delta modulation systems require high transmission rates to achieve comparable performance with PCM, but result in simpler hardware.

When comparing two different types of digital code it is necessary to consider their performance at the same bit-rate. A comparison of different types of DM and PCM showing signal to noise ratio as a function of output bit-rate is shown in Figure 1.11. It can be seen that at low bit rates, below 200 K bits/sec, DM gives better performance. As the signal to noise ratio is increased, the band-width requirements of DM become disproportionately greater.

The complexity of DM systems remains the same as the data-rate is increased because the number of functional components is constant. For PCM codecs using ladder network the amount of hardware increases with the number of bits. The performance of the coder is determined by the accuracy of the components in the ladder networks.

1.5.1 Code Conversion Techniques

The previous section outlined a number of digital systems which

employ different digital codes. Once a signal is in a chosen digital code, it is possible to convert it into a different code format using additional digital circuitry. Such systems, known as code converters, remove the need for signals to be converted back into analogue form and re-encoded into a different code format.

This report concentrates on code converters which change PCM into one-bit codes, such as delta modulation, which can be decoded easily into analogue signals. The digital output of a delta modulator only requires low-pass filtering to obtain an analogue output, in contrast with a PCM D/A converter which requires complex analogue circuitry. The justification for the code conversion from PCM to delta modulation arises from having eliminated analogue circuitry at the expense of providing additional digital hardware. Since digital hardware can be manufactured cheaply, an overall saving in production costs can be obtained.

The code converter described consists of a digital delta sigma modulator which functions in the same manner as its analogue counterpart. As the modulator contains a quantizer, it produces some additional noise and distortion, so in order to achieve a performance comparable with that of the PCM input, these must be reduced to an insignificant level.

1.5.2 Future Growth Areas

Digital systems have an obvious advantage over conventional analogue audio systems. Now that digital storage and transmission are available, it is possible to outline a digital Hi-Fi system. The basic system shown in Figure 1.12 is currently planned, and is due to be released in 1982/83. Most of the major components can be found in any Hi-Fi system today; the new digital hardware is offered as a compatible add-on unit. In the future, as the popularity of digital discs increases, a digital system would take the form shown in Figure 1.13. In such a system many of the functions currently found in analogue systems have been replaced by digital

hardware. It is practical to implement conventional tone filters in digital form, giving superior performance and the opportunity for overall control by micro-computer. The eventual replacement of the high quality VHF music broadcasting system by UHF digital radio data links would improve transmission quality, bringing it up to the standard of the compact disc.

All of these developments will depend on the cost of suitable D/A and A/D converters. Every system currently under review needs a D/A converter and a conventional power amplifier. Implicit in the D/A converter's structure are suitable filters to reconstruct the analogue signals.

If the D/A converter was replaced by a code-converter which produced a one-bit delta-sigma code, the only analogue component required would be in the low-pass filter, which filters the output of the dsm. Since the sample rate of the dsm is higher than the conventional D/A converter, the specification of the low-pass filter can be relaxed. Provided this was the case, the system shown in Figure 1.14 could be used. In such a system, the DSM data is used to switch a high voltage electronic switch feeding the loudspeaker. Since the loudspeaker is in effect a low-pass filter, a completely digital system could be developed, eliminating the need for any analogue processing.

1.6 Structure of this Report

This chapter has discussed the trend towards digital electronics in the audio Hi-Fi industry. It has shown the need for a cheap Hi-Fi digital to analogue converter; conventional converters have been discussed and shown to be expensive, since they require high-precision components. The use of code-converters which use delta sigma modulation has also been mentioned.

Chapter 2 examines basic linear DSM and its possible exploitation in the Hi-Fi D/A converter.

Chapter 3 shows how error feed-forward correction can be incorporated into the basic DSM to produce a working prototype capable of meeting a Hi-Fi specification.

A second generation of DSMs and their performance is outlined in Chapter 4. The whole digital system is assimilated in Chapter 5, where suitable digital tone filters are investigated. A practical all-digital amplifier is also described.

All the techniques discussed and results obtained, together with a review of an all-digital system, plus any future work required, are presented in the concluding chapter, Chapter 6.

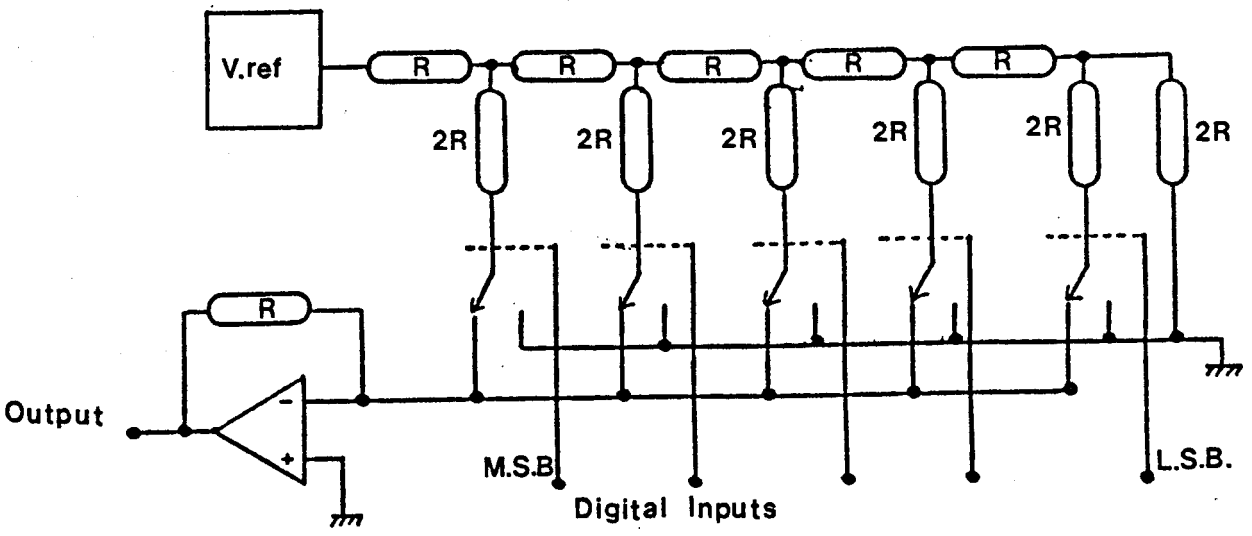


Figure 1.1 An R-2R ladder D/A converter.

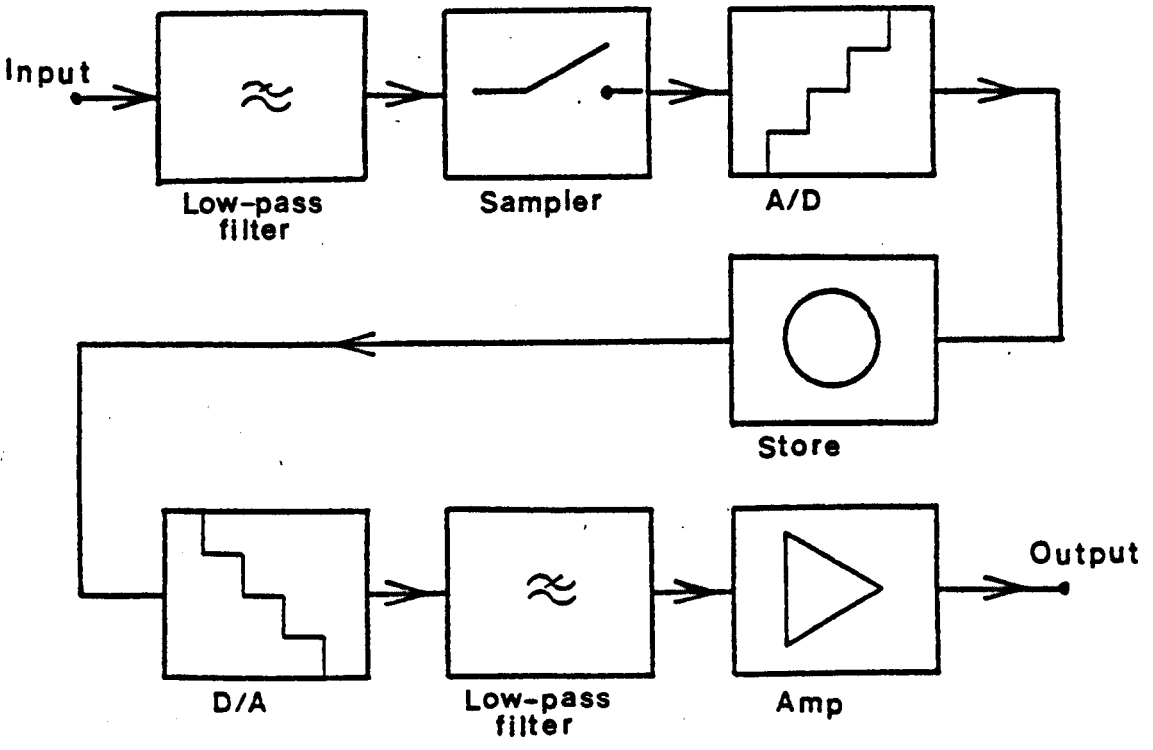


Figure 1.2 A generalized digital audio system.

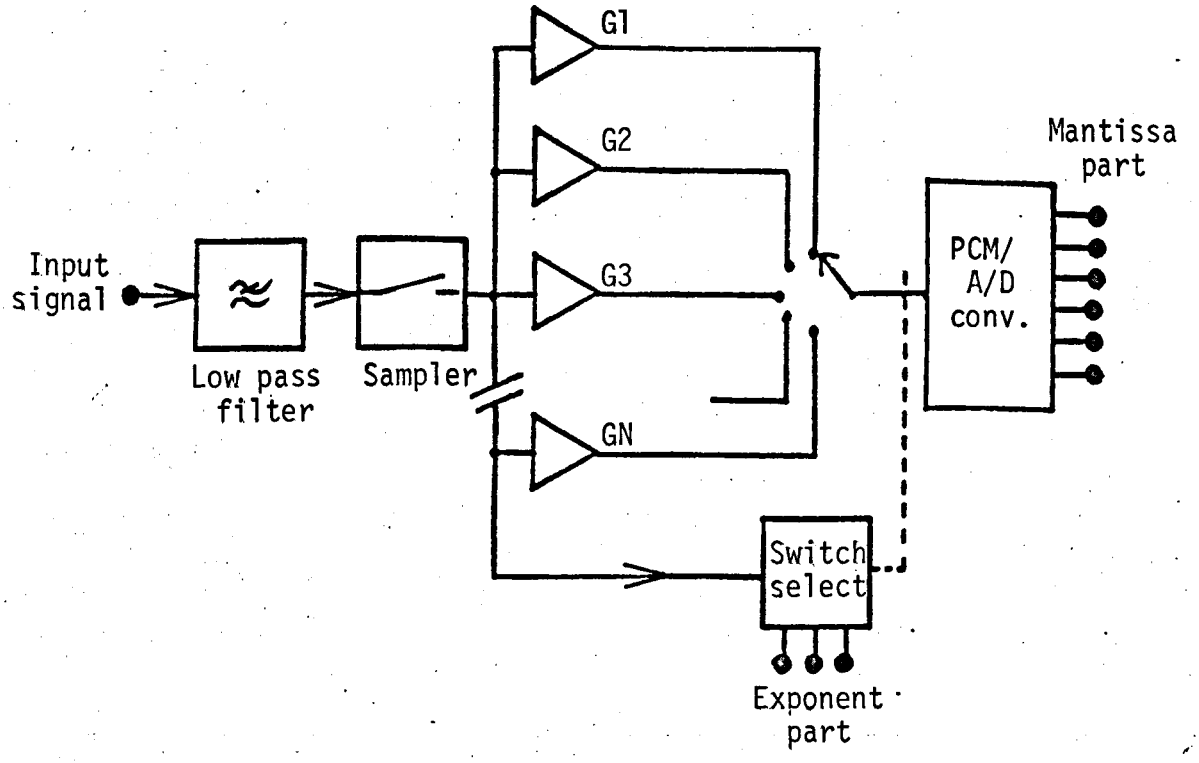


Figure 1.3 Block diagram of a general floating point A/D converter.

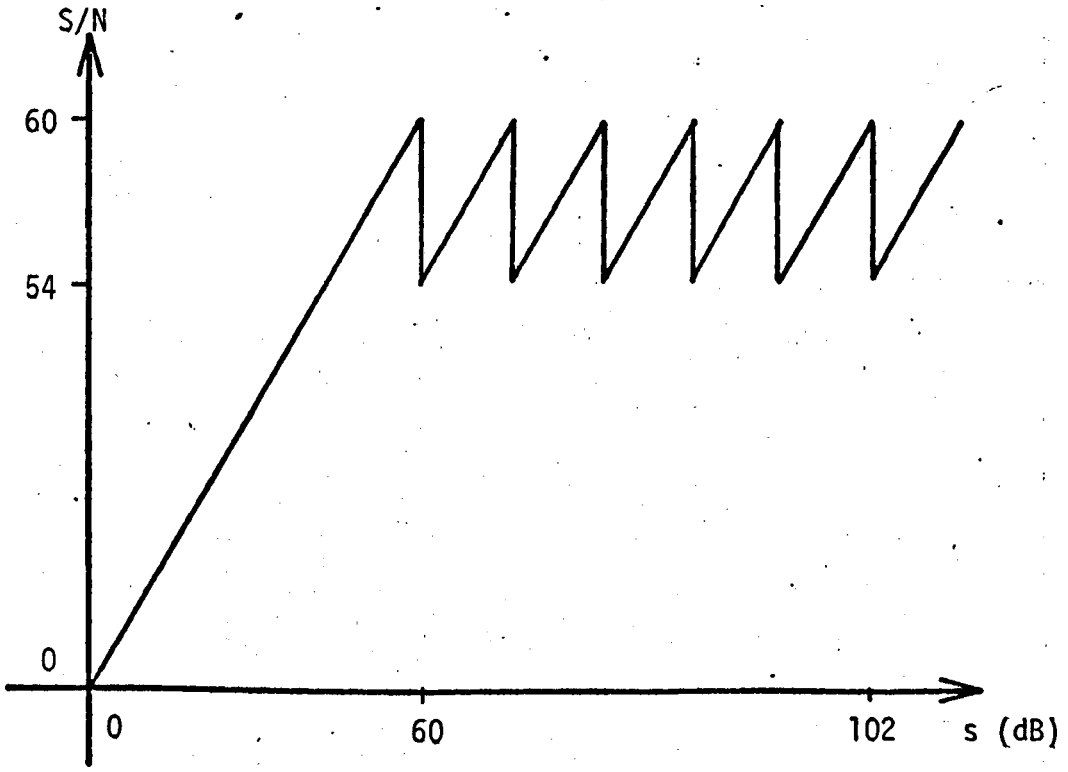


Figure 1.4 S/N for a floating point A/D converter with 10 bit mantissa and 3 bit exponent.

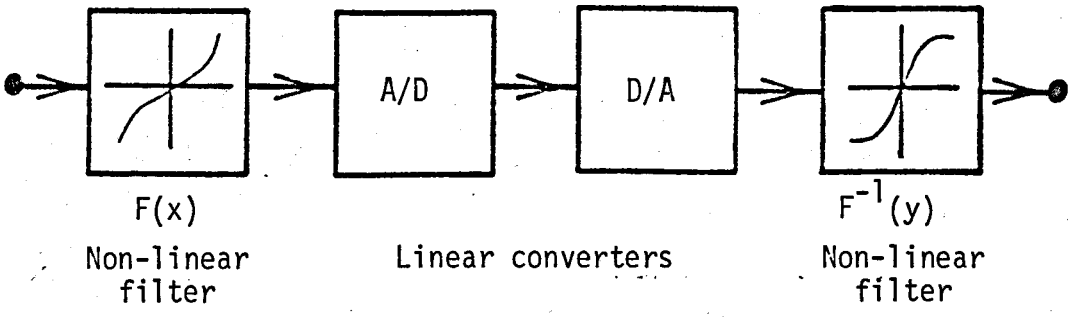


Figure 1.5 Model of a non-linear conversion system.

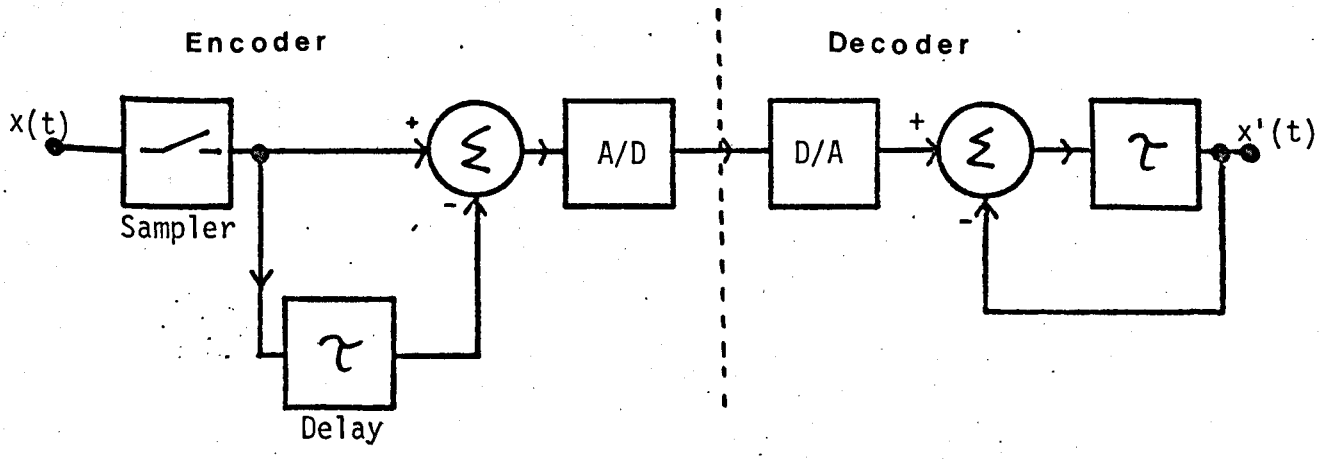


Figure 1.6 Differential P.C.M. system.

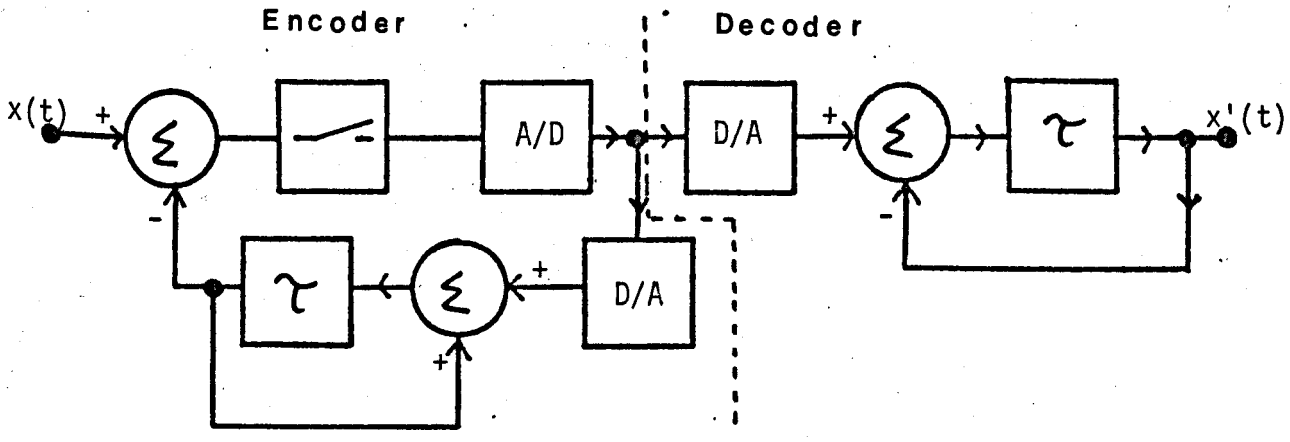


Figure 1.7 Modified differential P.C.M. system.

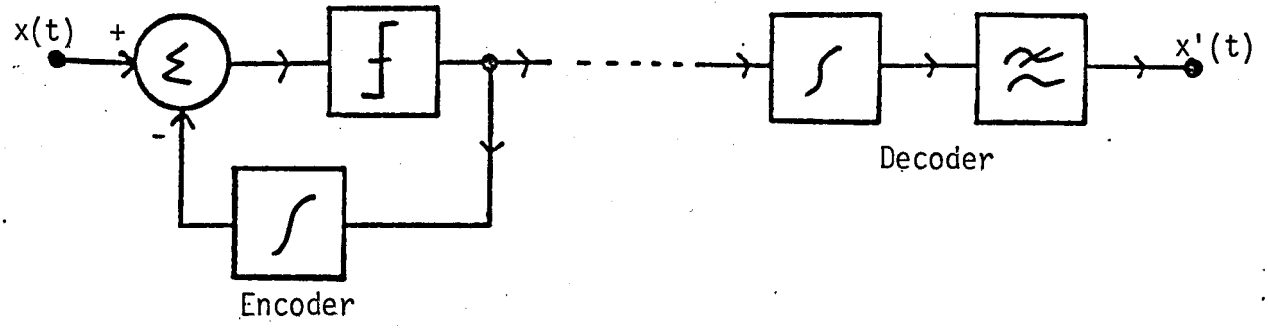


Figure 1.8 Delta modulator and demodulator.

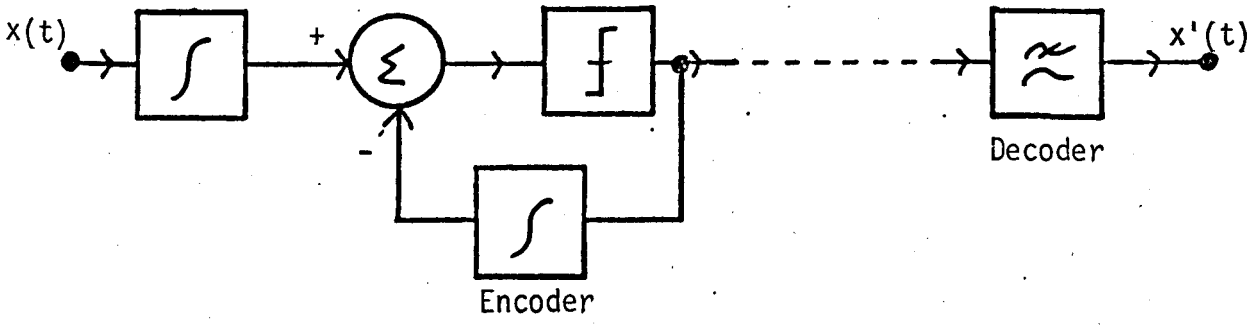


Figure 1.9 Conceptual model of a delta sigma modulator and demodulator.

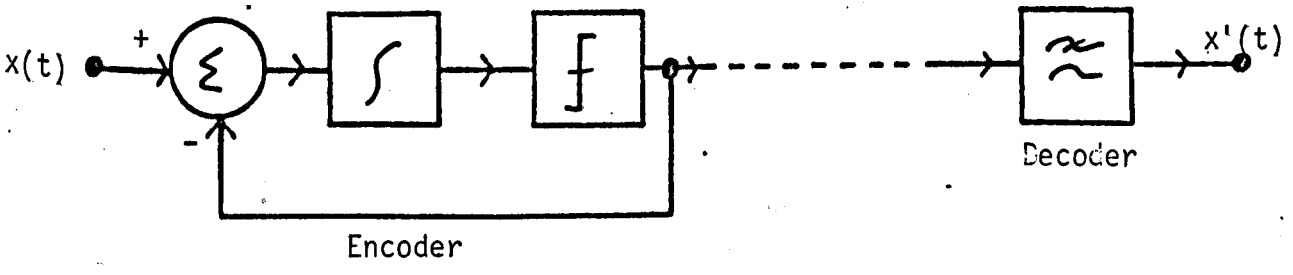


Figure 1.10 Practical realization of a delta sigma modulator and demodulator.

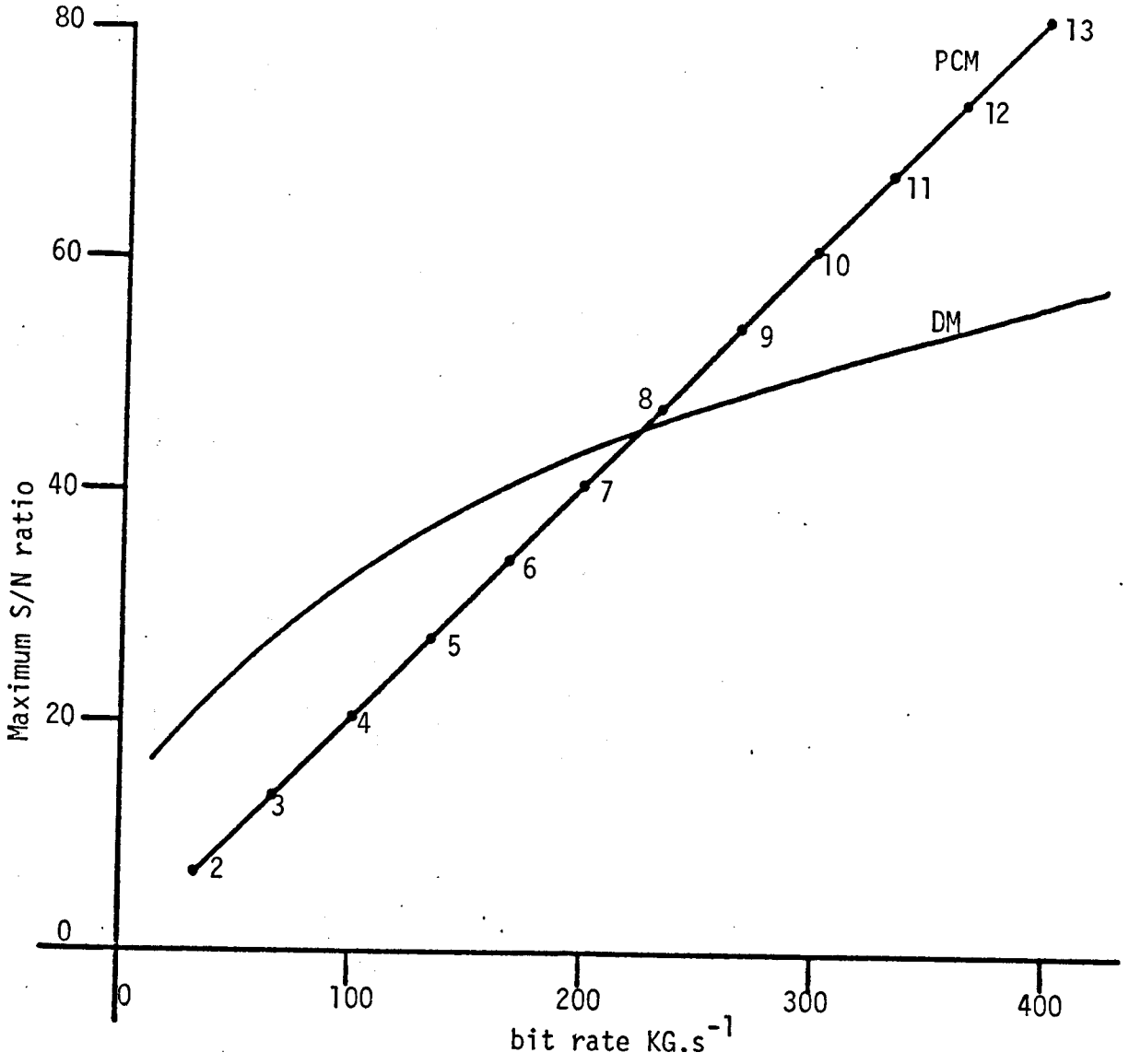


Figure 1.11 Comparison of the S/N of P.C.M. and D.M. at various bit rates for a 15 KHz system.

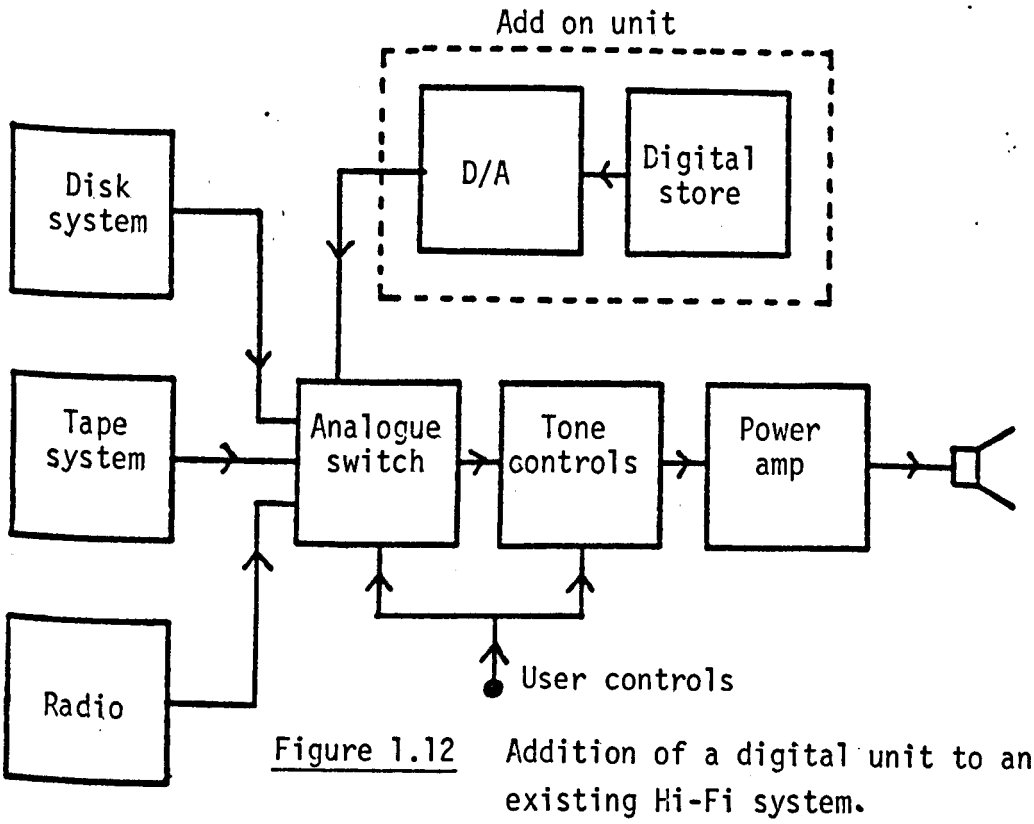


Figure 1.12 Addition of a digital unit to an existing Hi-Fi system.

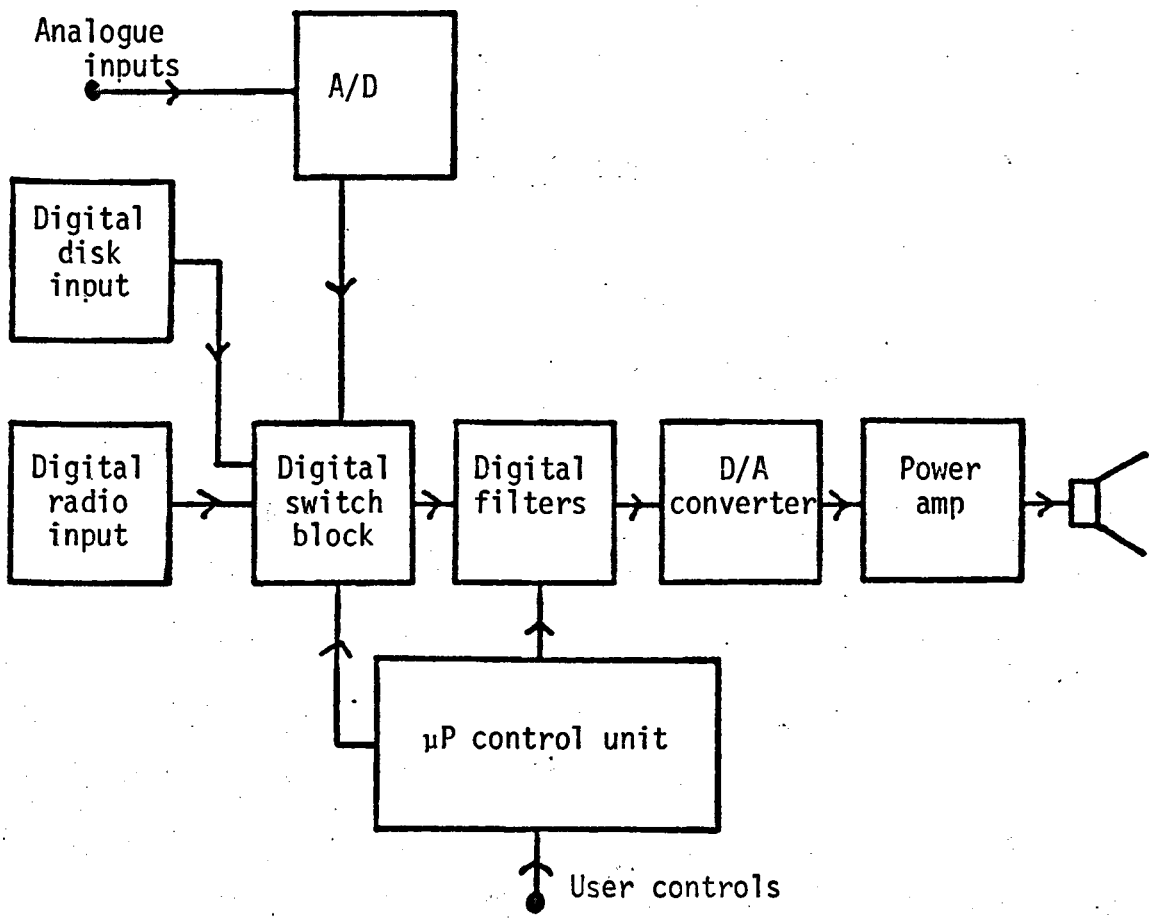


Figure 1.13 A possible arrangement for an all digital Hi-Fi system.

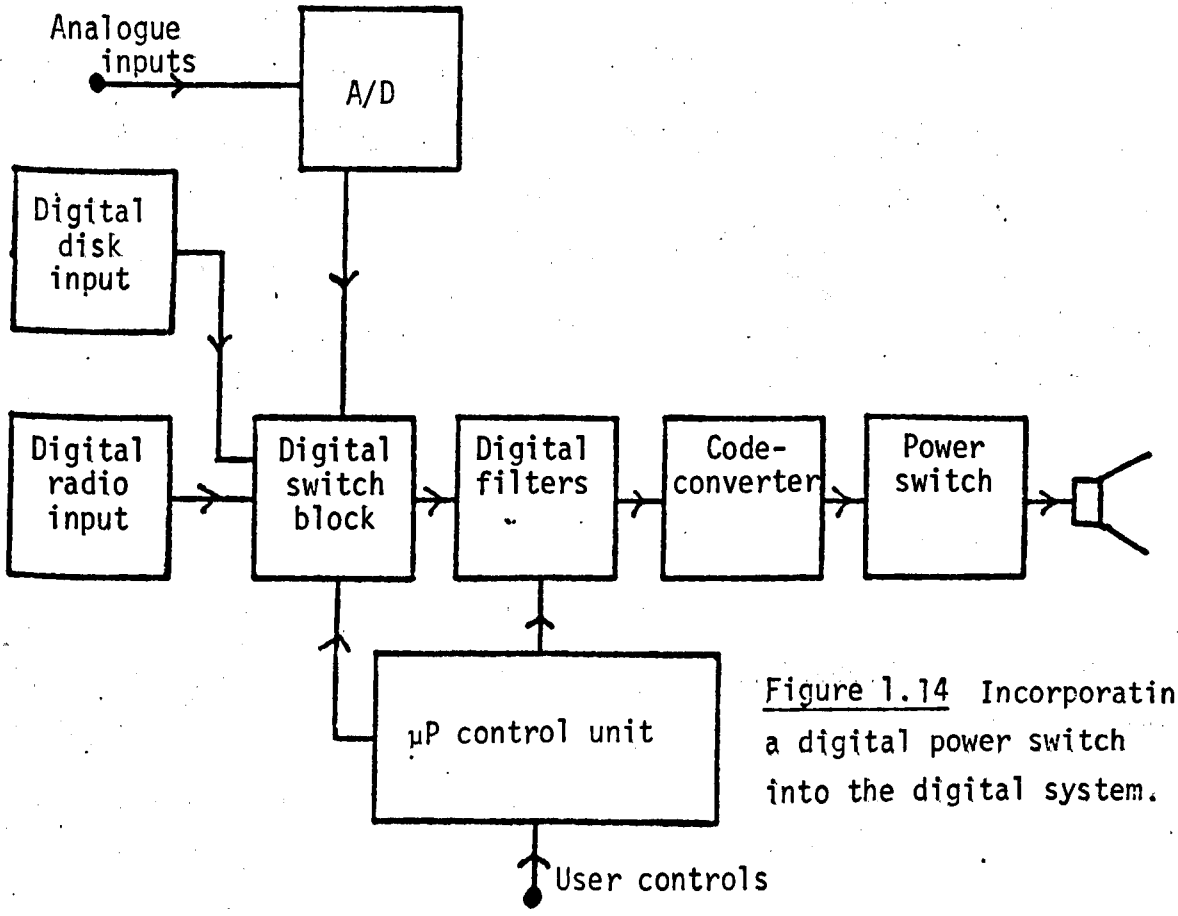


Figure 1.14 Incorporating a digital power switch into the digital system.

CHAPTER 2

FIRST ORDER DELTA MODULATORS

Up to this point the specification of digital audio systems and the types of digital codes used have been described. However, the success of any digital audio system in the domestic market will depend on its cost.

The technology required to produce current digital to analogue (D/A) converters for digital audio systems is not compatible with the mass production of low-cost consumer equipment. A D/A converter which did not require many analogue components, and which could be implemented on a single L.S.I. chip, would have a considerable economic advantage.

A digital P.C.M. signal consists of a number of digital samples which represent a close replica of the original sampled analogue signal. Provided sufficient samples of the analogue signal are taken, the fidelity of the digital signal is determined by the number of levels to which the digital signal is quantized. The number of quantized levels, which represent the original analogue signal, can be reduced if the amount of samples taken is increased well above the Nyquist rate, resulting in an over-sampled system.

Delta modulators are oversampled coders which produce a one-bit digital output signal. Of all the different types of delta modulators, delta sigma modulation (D.S.M.) has the simplest output code to decode. Decoding is accomplished by low-pass filtering the one-bit D.S.M. output to produce the required analogue voltage.

Using suitable digital circuitry, it is possible to convert between P.C.M. and D.S.M., thus enabling the multi-bit P.C.M. signal to be re-encoded into an over-sampled one-bit code, which can then be simply converted into

an analogue signal.

Provided that any additional noise introduced during conversion between P.C.M. and D.S.M. could be kept below acceptable limits, such a technique would enable the complex analogue structure of existing ladder network D/A converters to be replaced by an all digital code converter. If the necessary digital hardware could be placed on a single L.S.I. chip, then a considerable saving in the cost of D/A conversion would result.

The peak signal to noise ratio (S/N) of a linear D.S.M. can be calculated by using equation 2.1 (Appendix 1).

$$S/N = \frac{9}{8\pi^2}\left[\frac{f_m}{f_{s2}}\right] \qquad 2.1$$

f_m = Modulator clock frequency

f_{s2} = Highest input frequency

In order to give the same S/N as 14-bit P.C.M. at a 32 kHz sample rate, a D.S.M. would require clocking at 22 MHz. To enable production of the converter on a single L.S.I. integrated circuit, a clock rate below 10 MHz is desirable. The basic D.S.M. is therefore unsuitable for high quality systems at any practical clocking frequency.

Work by Candy, (Ref. 2.2) and Everard, (Ref. 2.3) shows how the performance of a D.S.M. can be enhanced by adding a small DC offset at the input to the D.S.M. Such a technique should enable a D.S.M. to be used successfully at a reduced clocking frequency.

To assess the improvement in performance of a D.S.M. resulting from the addition of a DC offset to the input signal, an initial series of experiments using an analogue D.S.M. was undertaken. The results obtained suggest that a digital D.S.M., when used as a code converter, could emulate the performance of 14-bit P.C.M. at realistic clock rates. Subsequent construction of the digital D.S.M. (D.D.S.M.) demonstrated some theoretical

limitations in the coder's performance and the need for some practical modifications. In the light of these observations, it is possible to assess the suitability of D.S.M. as an intermediate code in the conversion of P.C.M. into quality audio.

2.1.1 Analogue Delta Sigma Modulation

The D.S.M. as described by Inose and Yasuda, (Ref. 2.4) can be regarded as a linear delta modulator preceded by an additional integrator at the input. This enables the integrator in the decoder to be removed, resulting in a simple decoding structure. It also has the effect of modifying the peak-encoding characteristic, (derived in Appendix 1) so that the peak signal level, which can be encoded, becomes independent of frequency, an advantage when encoding music. As a result of achieving a flat overload characteristic, the threshold of encoding of the original delta modulator becomes modified and rises at 6 dB/octave; the quantization noise spectrum is modified in the same manner. These effects are summarised in Figure 2.1.

A function diagram of an analogue D.S.M. is shown in Figure 2.2, it only contains three main functional elements:-

1. Summer
2. Quantizer
3. Integrator

These functions can be implemented using two active components. The circuit shown in Figure 2.3 contains an operational amplifier configured as an integrator with the virtual earth also used to sum the approximation signal. The D-type flip-flop becomes the quantizer which is clocked at a rate higher than that of the Nyquist rate. This circuit was originally employed as part of a codec for use in telephony systems as described by Everard (Ref. 2.1).

2.1.2 Operation of an Analogue Delta-Sigma Modulator

The circuit of the d.s.m. shown in Figure 2.3 consists of a feedback loop in which the approximation signal (q(t)) is compared to the input signal (X(t)). The resulting difference (x(t) - q(t)), which is the error signal (e(t)), is integrated using the analogue integrating capacitor C_1 in the feedback circuitry of the operational amplifier. The integrated error signal is then presented to the D-type flip-flop. At the end of each clock period (T) the D-type is clocked and the sign of the integrated error signal at its input is used to control the sign of the approximation signal during the next clocking period.

The only values which q can take are +V and -V, where V is equal to the maximum input signal allowed. Suppose the integral proved positive, then +V would be used to create a negative difference which would push the integral towards zero. The bias voltage applied to the non-inverting input of the operational amplifier is set to $^{+V}/_{2}$ so the uni-polar output of the D-type can be converted to bi-polar form.

Since the output of the D-type is clocked at $\frac{1}{T}$ a new approximation signal can only be produced after a period T. As each new approximation signal is generated, the sign of the error signal ensures that the new value will cause the error signal to oscillate around zero. This is crucial to the correct operation, of the d.s.m., which restricts the magnitude of the error signal.

If the output of the d.s.m. is averaged over a period (P) of many clock periods, then the difference between the error signal at the beginning of the period (E(nT)) to that at the end (E(nT+P)) was shown to be (Ref. 2.1) given by:-

$$\frac{1}{P}\int_{nT}^{nT+P}(x(t) - q(t)\,dt) = \frac{E(nT+p) - E(nT)}{p} \qquad 2.2$$

where P = averaging period nT = start of the averaging period after n clock periods

Since the values of E(nT+P) and E(nT) are restricted by the loop, as P increases the R.H.S. of equation 2.2 tends towards zero, therefore:-

$$\frac{1}{P}\int_{nT}^{nT+P} x(t)\,dt \approx \frac{1}{P}\int_{nT}^{nT+P} q(t)\,dt \qquad 2.3$$

Thus the effect of the modulator is to cause the average value of the approximation signal to equal the average value of the input. To encode a bandwidth (B) the averaging period can be increased by increasing the clocking period.

2.1.3 Circuit Details of the Analogue D.S.M.

The two possible values for the approximation signal (q) are a "logic 1" voltage (V_1 = 3.7 V) and a "logic 0" voltage (V_0 = 0.2 V). Bi-polar operation is accomplished by setting the offset voltage to the mid-point of these two voltages

$$\text{Offset} = V_{os} = \frac{3.7 - 0.2}{2} = 1.95\ \text{V} \qquad 2.4$$

The output swing of the integrator is given by:-

$$\Delta V = \pm \frac{VT}{2\,C_1R_3} \qquad \text{where V = 5 V.} \qquad 2.5$$

It is necessary to make ΔV sufficiently large to overcome the D-type's hysteresis, typically 1 volt. If the input signal is zero, then the feedback path will ensure that the approximation signal will assume V_1 and V_0 in equal proportions to keep the mean current flowing into the summing junction at zero. This results in a stream of alternating "logic 1's" and "logic 0's", known as the idle channel pattern. For any signals below the overload point the stream of "logic 1's" and "logic 0's" will change to ensure that the mean current flowing into the summing junction is always zero. Under these conditions over the time period (P),

$$\frac{1}{P}\int_{nT}^{nT+P}\frac{q(t)}{R_3}\,dt = 2\,\frac{1}{P}\int_{nT}^{nT+P}\frac{x(t)}{R_1}\,dt \qquad 2.6$$

Overload will occur when there is a constant stream of "logic 1's" when:-

$$x(t)\Big|_{max} = \left(\frac{R_3}{R_1}\right) = V \qquad 2.7$$

The threshold of encoding is the level at which the input signal can no longer change the idle pattern. When idling the approximation signal is a square wave of amplitude ±V which after integration becomes a triangular wave of $\frac{\pm VT}{2}$.

If an input signal of the form $X\,\mathrm{Sin}(2\pi f_a t)$ is assumed, then its contribution to the output voltage of the integrator will be:-

$$\frac{-X\,\mathrm{Cos}\,(2\pi f_a t)}{2\pi f_a} \qquad 2.8$$

The encoding threshold will occur when this signal can no longer influence the idle pattern, i.e.:-

$$\frac{-X}{2\pi f_a} \leq \frac{VT}{2} \qquad 2.9$$

Substituting $x(t)_{max}$ from equation 2.7 and evaluating x_{min} from equation 2.9 the dynamic range (D) is given by:-

$$D = \frac{R_3 f_m}{\pi R_1 f_a} \qquad 2.10$$

f_a = signal frequency

f_m = modulator frequency

which is in the same form at the theoretical dynamic range derived in Appendix 1.

2.1.4 Performance of the Analogue D.S.M.

The practical results for the linear d.s.m. are summarised in Figure 2.4, which shows the theoretical and practical signal to noise

measurements. These results show that the analogue d.s.m. has a practical limit to the clock frequency of approximately 2 MHz; above this frequency the performance does not improve. This was found to be caused by slew-rate limiting in the operational amplifier.

However, restricting the operation of the circuit at 2 MHz the improvement in the performance of the modulator when a small D.C. offset is added to the input signal can be clearly seen in the results shown in Figure 2.5. The value of this D.C. offset was determined by experimentation and a description of the mechanism causing this improvement is given in Section 2.3.2. These results show that a D.C. offset can not only improve the low level performance by 10 dB but also extend the dynamic range by between 10-15 dB. The peak signal to idle channel noise is better than the observed dynamic range at 87 dB.

2.2.1 Digital Delta Sigma Modulator

Although the performance of the analogue d.s.m. is restricted by the low clocking rates possible, the improvement achieved by adding a D.C. offset show that a Hi-Fi system should be practical at an 8 MHz clock rate. The limitations in the analogue system, particularly in the design of the operational amplifier, make further development of the system impractical. Thus having established the validity of D.S.M. as an intermediate code for D/A conversion, it is now practical to consider a digital code converter which re-encodes P.C.M. into D.S.M.

2.2.2 Operation of a Digital D.S.M.

As a d.d.s.m. consists of logic circuits its frequency limit is determined solely by the propagation delays of the logic elements. Typically this is 30 MHz for T.T.L. circuits. So a d.d.s.m. can operate satisfactorily at 8 MHz.

The operation of the d.d.s.m. is similar to the analogue system previously outlined and follows along the lines suggested by Everard (Ref. 2.1).

A functional diagram of the d.d.s.m. is given in Figure 2.6. As in the analogue system, the approximation signal (q(n)) can only take two possible values ±V. This is subtracted from the input signal (X(n)) to produce an error signal (e(n)). A digital accumulator integrates this error signal, by adding it, at the end of clock period n to the summation of all previous errors (I(n)), forming the new accumulated error (I(n+1)). Hence:-

$$I(n+1) = I(n) + e(n) = \sum_{i=0}^{i=n} x(i) - q(i) \qquad 2.11$$

The sign of I(n+1) is used to control the approximation signal, which is then subtracted from the next input, its sign being chosen to minimise the next error signal:-

$$q(n+1) = V \quad \text{sgn}\left[I(n+1)\right] \cdot \quad \text{where:-} \qquad 2.12$$

$$\text{sgn}\,|x(i)| = 1 \quad x \geq 0$$

$$= -1 \quad x < 0$$

This feedback path results in the accumulated error tending to zero, indicating correct d.s.m. operation. The input signal is sampled and held for m D.S.M. clock periods, therefore the D.S.M. clock frequency is related to the input signal's sample frequency by:-

$$f_m = m \cdot f_s \qquad 2.13$$

f_m = D.S.M. clock frequency

f_s = P.C.M. sample frequency

Averaging over the period of m D.S.M. clock periods:-

$$\frac{+1}{m} \sum_{i=n-m}^{i=n} x(i) = -\frac{1}{m} \sum_{i=n-m}^{i=n} q(i) - \frac{1}{m} \left(I(n) - I(n-m)\right) \qquad 2.14$$

Hence, the average input signal is equal to the average approximation signal, plus some average error signal. The longer m is, the greater the number of approximations to the input signal produced, and the smaller the error signal becomes. However, according to equation 2.13 the longer m

becomes, the greater the modulator clock frequency.

By providing an additional adder at the modulator's input, the effect of adding a fixed offset to the P.C.M. input signal can be investigated.

2.2.3 Circuit Details of the Digital D.S.M.

The circuit of the digital D.S.M. is given in Figure 2.7. The 14-bit P.C.M. input is first added to the required offset in the first input adders. To avoid corruption to the sign-bit when the offset is added to peak signals, a limiter is provided by detecting the sum of the offset and input signal. If overload was to occur, the signal is pre-set by the set of AND gates to the maximum allowed. The resulting signal is applied to the lower 14 bits of a 15-bit accumulator, made up of full adders and D-type flip-flops. An additional one-bit feedback path is introduced by inverting the output of the most significant D-type. This signal is then connected to the most significant input of the accumulator to form the approximation signal, which is also the D.S.M. output. Using the 15-bit of the accumulator, the M.S.B., as the approximation signal, eliminates the need for additional hardware, which is normally necessary to add the approximation signal. This is possible because the number range used within the system is in offset binary form. The range of possible input signals is $0 \leq X \leq 2^{14} - 1$, and the approximation signal can have either of the two values of 0 and 2^{14}. Then taking the 15^{th} bit of the accumulator gives the required quantized approximation signal. This reduces the possible dynamic range of the input signal by an insignificant amount. Since the accumulator is not re-set each time a new input signal is clocked in, the accumulated error is carried over into the next sample period as required.

2.2.4 The Effect of Finite Slopes in the D.S.M.'s Output

The analogue output of a d.d.s.m. is produced by low-pass filtering

the logical data stream which represents the approximation signal. Within the digital modulator this signal is considered ideal with infinitely short rise (τ_r) and fall (τ_f) times. It has been observed experimentally that differences in the rise and fall times of the output signal results in the generation of additional noise at the modulator's output. It is instructive to determine why additional noise is produced and how it can be minimized. An initial understanding of the mechanism which produces this noise can be gained by considering DC signals only. For this type of signal the modulator's output voltage is proportional to the average area of the periodic pulse pattern. In this case the actual output voltage is dependent on the number of "logic 1"'s which occur over the averaging period.

In the negative half of the DC transfer characteristic, the D.S.M. ensures that each "logic 1" is separated by at least one "logic 0". Thus the density of single "logic 1"'s increases as the required output voltage approaches zero. At zero input an alternate pattern of one's and zero's, the idle pattern, is produced. For positive signals, each additional "logic 1" will occur alongside existing pulses, thus blocks of multiple "logic 1"s are formed.

If the output signal consists of pulses with infinitely short rise and fall times, then the change in area resulting from inserting an additional pulse, adding a pulse between two "logic 1"'s or alongside an existing "logic 1" will be identical. Therefore the output voltage is solely a function of the density of pulses produced.

In practice, the modulator's output will be provided by a TTL totem pole gate which will have finite and different rise and fall times (Ref. 2.5). This results in a change in the contribution made by each additional "logic 1" depending on its position relative to the existing pulse pattern. There exist three possible positions where an additional pulse could be inserted:- between two "logic 0"s changing the average area by A_{vn}; between two "logic 1"s changing the average area by A_{vo}; or by

extending a simple single "logic 1" to form a pair, thus changing the average area by A_{ve}. All these conditions are illustrated in Figure 2.8 where the respective increases in area are shown to be :-

$$A_{vn} = 1 - \tau_r + \tau_f \qquad 2.16$$

$$A_{vo} = 1 - \tau_f + \tau_r \qquad 2.17$$

$$A_{ve} = 1 \qquad 2.18$$

It is possible to investigate the D.C. transfer characteristic for a D.S.M. by using a computer to simulate all the possible pulse patterns and to take into account the finite rise and fall times. A suitable programme is included (EDGES) in Appendix A4.8. This programme superimposes linear rising and falling edges on an ideal 7-bit D.S.M. wave-form and calculates all the new output voltages. The results of this simulation are displayed in Figure 2.9, which shows the transfer characteristics produced for different rise and fall times. It can be seen that with unequal rise and fall times the transfer characteristic consists of two different linear regions, one for the positive quadrant and one for the negative quadrant. The linear relationship between single pulse density (equation 2.16) and output level in the negative quadrant shown in Figure 2.9 is predicted by equation 2.19, where K= density of pulses.

$$V_{out}(V_{in} \leq 0) = KA_{vn} \qquad 2.19$$

However the increase in area associated with forming groups of odd or even numbered pulses is different (equations 2.17 and 2.18) and as these groups are only produced for positive signals, a linear relationship between pulse density and output voltage in the positive quadrant is unexpected.

Inspection of the groups of pulses produced by a D.S.M., over a entire output period, shows that groups containing even numbers of pulses are only produced in even numbers, while the number of groups containing odd numbers of pulses can only be 2,5,8,11 etc. This is because certain

groups of pulses are equivalent i.e. a pair of double pulses is equivalent to a single triple pulse when averaged over a complete period. A D.S.M. attemps to produces the maximum number of transitions, thus producing a pair of double pulses, not a single triple pulse. However, in general by comparing different pulses with identical areas it is convenient to consider the real even groups of pulses which occur as equivalent to the odd groups that do not occur. Therefore it is also possible to represent the positive transfer function as:-

$$V_{out}(V_{in} > 0) = KA_{vo} \qquad 2.20$$

If the rise and fall times of the pulses are made equal then equations 2.16, 2.17 and 2.18 all simplify to unity. This permits the important observation that the significance of inserting additional pulses with equal rise and fall times into a stream of data is unaffected by the position of the existing pulses. An important first step in reducing the additional noise caused by the finite rise and fall times of the practical pulse pattern is to ensure that it has equal rise and fall times.

A more comprehensive simulation programme (SPECTRUM) was produced to determine accurately the additional noise power produced by finite width transitions. The true output signal can be considered as containing two components, the ideal output signal and an additional error signal resulting from the finite transitions. Figure 2.10a shows a typical output signal . The ideal waveform is illustrated in Figure 2.10b and the error signal in Figure 2.10c. If a 7-bit D.S.M. clocked at 4096 KHZ and encoding a 500 HZ signal, is considered, then a maximum of 16384 possible transitions could occur in the periodic output sequence. This precludes the possibility of calculating the Fourier transform of the sequence directly. Similarly, to produce an FFT of the error signal, the number of data points would need to be increased to approximately 163K points to provide the required resolution, requiring large amounts of computer time. An

alternative approach is possible because the error signal only contains two components, a rising edge and a falling edge; these two are subsequently shifted in time and repeated. Since it is possible to calculate the displacement in time of each rising and falling edge, the superposition theory can be used to calculate the total in-band noise once the spectrum of the two edges is known. To calculate the Fourier transform of the rising and falling edges, they are assumed periodic at the signal frequency (T) and occur at t=0; they then take the form of equations 2.21 and 2.22. for a rising edge; where T= period of the input signal, n= harmonic number.

$$f(\omega) = \frac{-1}{T}\left(\frac{1}{jn\omega} + \frac{1 - e^{-jn\omega\tau_r}}{\tau_r n^2\omega^2}\right) \qquad 2.21$$

for a falling edge;

$$f(\omega) = \frac{1}{T}\left(\frac{1}{jn\omega} + \frac{1 - e^{-jn\omega\tau_f}}{\tau_f n^2\omega^2}\right) \qquad 2.22$$

The frequency domain components of these waveforms are modified by the shift in time to their actual positions in the modulator's output by multiplying each term by the corresponding term in equation 2.23 below, where $p\tau$= shift in time, τ= modulator's clock period.

$$f(t + p\tau) \longrightarrow e^{-jn\omega p\tau}.f(\omega) \qquad 2.23$$

Using this method, the frequency spectrum resulting from each transition in the periodic output sequence of a modulator can be calculated. If all the individual in-band components are summed, the total in-band noise produced by the finite transitions can be obtained. To enable a simulation programme to be written it is necessary to arrange equations 2.21, 2.2 & 2.23 in a convenient form, by relating $T, p\tau, \tau_f, \tau_r$, and n the following are found to be true.

For a rising edge; where $\omega_r = n\,\tau_r$, with τ_r a fraction of T:

$$V_r = \frac{\cos(\omega_r) - 1}{\omega_r . n . 2\pi} + j\left(\frac{1}{n . 2\pi} - \frac{\sin(\omega_r)}{\omega_r . n . 2\pi}\right) \qquad 2.24$$

For a falling edge; where $_f = n\,\tau_f$, with τ_f a fraction of T:

$$V_f = \frac{1 - \cos(\omega_f)}{\omega_f . n . 2\pi} + j\left(\frac{\sin(\omega_f)}{\omega_f . n . 2\pi} - \frac{1}{n . 2\pi}\right) \qquad 2.25$$

For the delay term; where $\omega = 2\,\tau/T$, with p=position of edge:

$$V_d = \cos(\omega . n . p) + j\,\sin(\omega . n . p) \qquad 2.26$$

The results of simulating an output pulse pattern with equal rise and fall times are displayed graphically in Figure 2.11. It can be seen that with no rise or fall times the additional distortion produced is equal to the background noise of the program, at -160 dB. Subsequent increases in the edge times result in an increase in the amount of distortion produced although this levels out at approximately -100 db. The levels of distortion produced for unequal rise and fall times are typical of those obtained in practice. They show an increase in the distortion produced when the rise time is assumed zero and the fall times are changed between 0-20% in Figure 2.12a, and 0-100% in Figure 2.12b. Other combinations such as a rise time of 10% and fall time of 20% give results approximately equal to those shown for a 10% difference. These results can be used to determine the amount of distortion produced by a known difference in the rise and fall times of an output signal. These results can be interpreted as showing two different effects. Large, unequal edges in the pulse pattern produce significant even harmonic distortion . This is consistent with the analysis made on the transfer characteristics. When periodic signals are considered the energy contained in the finite edges of the output pulse pattern is distributed within a line spectrum, where the line spacing is related to the period of

the input signal. The primary complex line spectrum of the rising and falling pulses at t=0, are complementary only if the rise and fall times are equal. These spectra become unique when they are modified by the time shift function (equation 2.23) however the results demonstrate that cancellation of the individual complex lines occurs. In practice a residual line spectrum occurs which is relatively independent of the primary line spectra, whenever the rise and fall times of the pulse pattern are equal or similar. The simulation has only tested a D.S.M. system over one period of output data, however in practice the pattern produced would extend over a longer period but it is considered representative of the real system.

The importance of maintaining equal rise and fall times on the edges of the output pulse pattern has been shown; furthermore the significance of equal edges also producing distortion has been quantitatively investigated. This has lead to the observation that the distortion produced by finite edges would limit the system's performance representing a fundamental limitation in more accurate systems.

2.2.5 Correction of the Output Signal's Edge Slope

The analysis in the previous section showed how imbalance in the D.S.M. output affected the overall performance. At clock rates of 4096 x 10^3 Hz, negligible distortion would be introduced using standard T.T.L. circuits. In practice the rise and fall times are increased when the output gate drives a highly capacitive load, such as a low-pass filter.

L.S.I. circuits are built with components which cannot be critically matched, so such circuits require careful design to ensure that the overall performance is independent of component tolerances. To reduce the modulator's sensitivity to unequal rise and fall times, a differential circuit was developed to cancel this effect. This is shown in Figure 2.13.

2.2.6. Output Circuits Producing Signals Independent of Edge Imbalance

Two identical signals in anti-phase are produced by two D-type flip-flops, which re-time the D.S.M. output (y(t)) and the inverted output

($\overline{y}(t)$). This is necessary to remove any delay introduced by the single inverter. Every time a transition occurs in the output data, a rising and falling edge is presented to the input of the differential amplifier; consequently its output will be independent of any differences in these edges. As the frequency of the D.S.M. output is around 8 MHz, some pre-filtering is necessary to allow the differential amplifier to function correctly. This pre-filtering is provided by the simple R.C. filters comprising of C_1 R_1. Their time constant is a compromise between the resulting in-band droop, which affects the coder's frequency response, and their high frequency attenuation which determines the required frequency response of the differential amplifier. Satisfactory matching is obtained by using 1% components. Additional trimming, effected by artificially changing the output slope of one D-type with the trimmer V_{C1} produced no improvement and was considered unncessary.

2.2.7 Performance of the Digital D.S.M.

Assessing the performance of high quality D/A converters is difficult since a suitable signal source must be obtained. Using analogue signal generation and an A/D converter to produce the required P.C.M. test signals causes problems in separating the noise produced by the encoder from that produced by the converter under test. These problems were overcome by using a micro-computer which outputs suitable data from memory. An outline of this system and the types of tests carried out is given in Appendix 2.

The measurements of signal to noise ratio over a range of different input signal levels confirms the theoretical predictions made in Section 2.1. Good agreement between theoretical calculations and practical results is obtained over the range of clock frequencies and signal levels tested, as displayed in Figure 2.14. Examples of the quantization noise spectrum, and of harmonic distortion introduced by the coder, are illustrated in Figure 2.15.

Employing digital D.S.M. useful measurements of the changes in performance resulting from the addition of D.C. offsets can be made. This was not possible using the analogue system, as the required D.C. stability and high frequency performance could not be obtained.

2.3.1 The Effect of D.C. Offsets on the Performance of the Coder

The pilot experiment, outlined in Section 2.1.1 showed that a small D.C. offset permanently added to the D.S.M.'s input signal results in an improvement of the modulator's performance.

The digital D.S.M. developed in Section 2.2.1 can be adapted to add any fixed D.C. offset required to the incoming digital signal. With this equipment it is possible to test the changes in performance due to a variety of different levels of applied D.C. offset.

2.3.2 Theoretical Consideration of a D.C. Offset's Effect on the D.S.M.'s Performance

With no input signal applied, the D.S.M. will produce the idle pattern 10101010 etc.. When a small D.C. signal is applied at the input of the D.S.M. shown in Figure 2.7, it will initially be clocked into the empty accumulator. However, during successive D.S.M. clock cycles, the level contained within the accumulator will increase. This will not affect the idle pattern until the accumulated sum equals the quantization thresholds, which are equal to the approximation signal (V). When this occurs, an extra "logic 1" will be introduced into the idle pattern and the accumulator will be re-set. The frequency at which this occurs will be related to how many D.S.M. clock cycles are required before the accumulated sum equals the approximation signal; for small signals this is given by:-

$$f_d = \left|\frac{V_{DC}}{V}\right| f_m \qquad 2.27$$

V = Approximation signal

f_d = fundamental frequency of disturbance

V_{DC} = applied DC input

This shows that the frequency of additional "logic 1's" falls as the input signal level is reduced. Although the average output of the modulator under these circumstances is correct, the frequency at which an additional "logic 1" occurs can fall below the cut-off frequency of the output filter (f_{max}). When this happens, the required signals are accompanied by considerable inband noise. The frequency at which this takes place can be calculated using Equation 2.27. The cyclic pattern produced by a 14-bit D.S.M. clocked at 8 MHz contains in-band noise components at signal levels below -55 dB. Equation 2.27 suggests a strong correlation between the amplitude probability density function, (P.D.F.), of the input signal, and the spectral distribution of the quantization noise power (Ref. 2.1).

The P.D.F. of a sinusoid is shown in Figure 2.16a. It can be seen that there is a significant probability of low level signals occurring. When such a signal is applied to a D.S.M., the noise spectrum, (shown in Figure 2.17a) contains significant low frequency components.

The P.D.F. of a sinusoid changes to that shown in Figure 2.16b when a small fixed D.C. offset is added; hence the probability of low level signals occurring is reduced. If this signal is applied to a D.S.M., the amount of low frequency quantization noise produced is correspondingly reduced. This is confirmed in Figure 2.17b. Thus the low frequency quantization noise, which would normally be produced when a low level input signal is encoded by a D.S.M., is shifted out of the message band when a small D.C. offset is added, so increasing the S/N.

Low-level signals which would normally be below the encoding threshold can be encoded when a D.C. offset is applied, since the offset ensures that the input signal can influence the idle pattern. This is best illustrated by considering the D.S.M. as a delta modulator preceded by an integrator. The result of applying a fixed D.C. to the input of this integrator is the generation of a ramp at its output, which would theoretically continue to grow indefinitely. A ramp will continually

pass through all the available quantization levels in the D.M., so any signal superimposed on this ramp will affect the point when these levels are crossed, thus enabling low-level signals to be encoded. Since the integrator is enclosed in the feedback path of the D.S.M. the maximum amplitude of the ramp is limited once it reaches the level of the approximation signal when it is reset.

Addition of the D.C. offset limits the dynamic range slightly since clipping occurs at a lower signal level.

An undesirable effect of the D.C. offset occurs when input signals cancel the applied offset. The P.D.F. of a sinusoid whose amplitude equals the proposed offset contains some low amplitude signals, as shown in Figure 2.16c. Figure 2.16d shows the change in P.D.F. when a D.C. offset is added. Now the probability of low level signals occurring has increased, which results in an increase in the amount of low-level quantization noise generated by the coder. This effect is demonstrated in Figure 2.17c.

The increase in low signal-level performance of the D.S.M. due to the addition of a D.C. offset is at the expense of the coder's high level performance. As signals cross the level equal to the applied D.C. offset, they generate bursts of low frequency quantization noise. This produces a dip in the signal to noise characteristic.

The non-encoding band, which is normally centred around zero in a D.S.M. with no D.C. offset applied, is shifted to a different point on the transfer characteristic when a fixed D.C. offset is applied. This occurs when:-

$$x(t) + d = 0 \qquad d = \text{applied offset} \qquad 2.28$$

The amount of noise introduced by the "dead band" in the transfer characteristic will depend on the P.D.F. of the input signal. The addition

of a D.C. offset will only give an improvement in perceived performance if the input signal has a high probability of remaining around zero.

2.3.3 Experimental Results Obtained using D.C. Offsets

It is possible to test the validity of equation 2.28 by plotting the signal to noise characteristics for a number of different D.C. offsets.

A set of experiments was carried out using seven different D.C. offsets at multiples of 6 dB below the peak level of input signal which equals each D.C. offset used; these results are tabulated below:-

Offset added at Bit Number	Equivalent input signal level
Bit 1 = M.S.B. = Sign Bit	—
2nd Bit	-6 dB
3rd Bit	-12 dB
4th Bit	-18 dB
5th Bit	-24 dB
6th Bit	-30 dB
7th Bit	-36 dB
8th Bit	-42 dB

The results of the signal to noise measurements for each offset are shown in Figure 2.18a to Figure 2.18g. They each show dips in performance at the predicted level of input signal. Offsets below the 3rd bit result in the predicted increase in low level signal performance. The offset which gives the most acceptable results appears to be positioned around the 4th bit, this value gives the required increase in low-level performance while only requiring peak signals to be reduced by 0.6 dB.

The quantization noise spectrum of D.S.M. rises with frequency so an increase in S/N may be obtained by using a de-emphasis filter on

the decoder. Other investigators have experimented with pre- and de-emphasis on P.C.M. systems (Ref. 2.6) but have shown that the resulting reduction in high-frequency dynamic range cannot be justified. Experiments carried out using an 80 μs de-emphasiser network and a D.C. offset give S/N results comparable with 14-bit P.C.M., see Figure 2.19a. This increase in observed S/N of 12 dB is at the expense of a reduction of 9 dB in the high frequency dynamic range, giving an overall improvement of 3 dB.

The frequency response of the coder without de-emphasis is shown in Figure 2.19b; the attenuation of 3 dB at the band edge is due to the $\frac{\sin x}{x}$ response caused by the sample and held input signal.

2.3.4 Perceived Performance

To assess the coder's performance at decoding music, a series of listening tests were carried out. Although these tests showed that the low level performance of the coder was comparable with 13-bit P.C.M., high level signals were accompanied by considerable program modulated noise. This noise was found to occur whenever signals passed through the dip in the S/N characteristic previously shown to be caused by the D.C. offset. This effect is clearly demonstrated in Figure 2.20, which shows a sinusoidal signal whose peak amplitude equals the applied D.C. offset. A burst of in-band quantization noise can be clearly seen occurring each time the input signal peaks cancel the effect of the applied D.C. offset. Since this noise is related to the input signal frequency, its presence is clearly audible above the background quantization noise.

2.3.5 A.C. Offsets

Applying a D.C. offset at the coder's input to redistribute the in-band noise results in a permanent D.C. offset on the coder's output. The same spectral re-distribution will occur if an A.C. offset is applied. If the frequency of the A.C. offset is equal to the input sampling frequency, then no additional in-band frequency components will be generated.

Experiments have shown no difference in the coder's performance with an A.C. offset applied. These results are summarized in Figure 2.21.

2.4.1 Concluding Remarks on First Order Systems

The digital coder described in this chapter had enabled an accurate assessment of the performance of a D.S.M. to be made.

The basic D.S.M. with no offset added to the input, performed according to the accepted theoretical predictions.

The improvements in the low signal level performance obtained by using a D.C. offset have been investigated and an optimal level selected.

Additional circuitry has been developed to eliminate the effects of finite rising and falling times on the output signal of the D.S.M.

Measurements on the performance of the optimised coder gives S/N results comparable with 13-bit P.C.M. However, tests using music have shown that considerable program-modulated noise is produced by the input signal, so cancelling the effect of the applied D.C. offset. Limitations in using an offset to redistribute the noise spectrum of a D.S.M. have thus been demonstrated.

When a D.S.M. with applied D.C. offset is used with a companded input signal, the effects of the dip in S/N which occur at high signal levels, are masked by the companding characteristic. Thus D.S.M.s of the type described are suitable in companded systems, as their low signal performance is good and they have a good peak to idle channel noise. It is unlikely that this type of D.S.M. could give 14-bit P.C.M. performance at clock rates below 10 MHz.

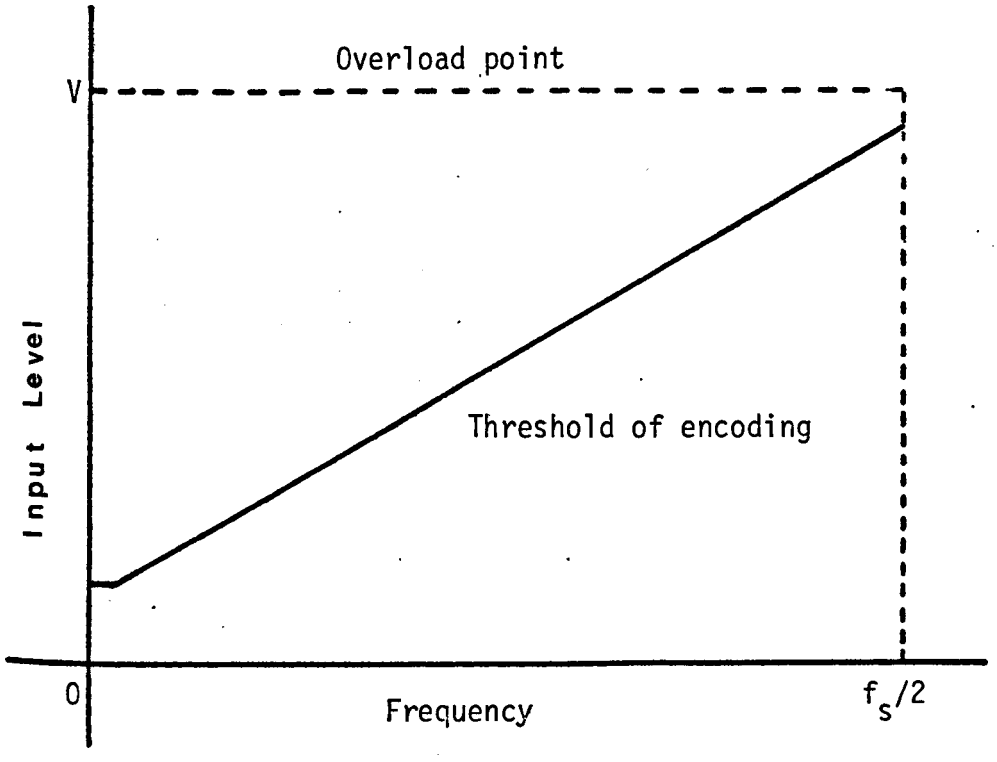


Figure 2.1 Display of d.s.m. characteristic showing the threshold of encoding and overload point as a function of modulating frequency.

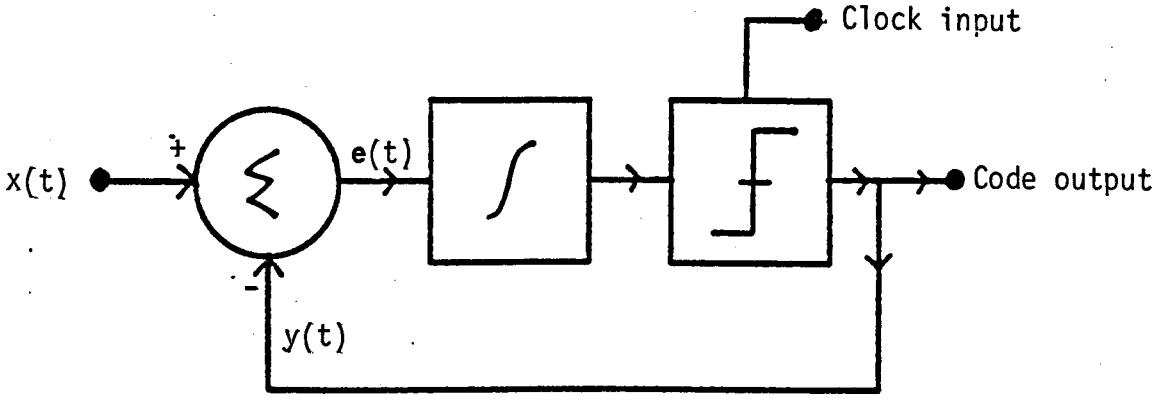


Figure 2.2 Functional diagram of a d.s.m.

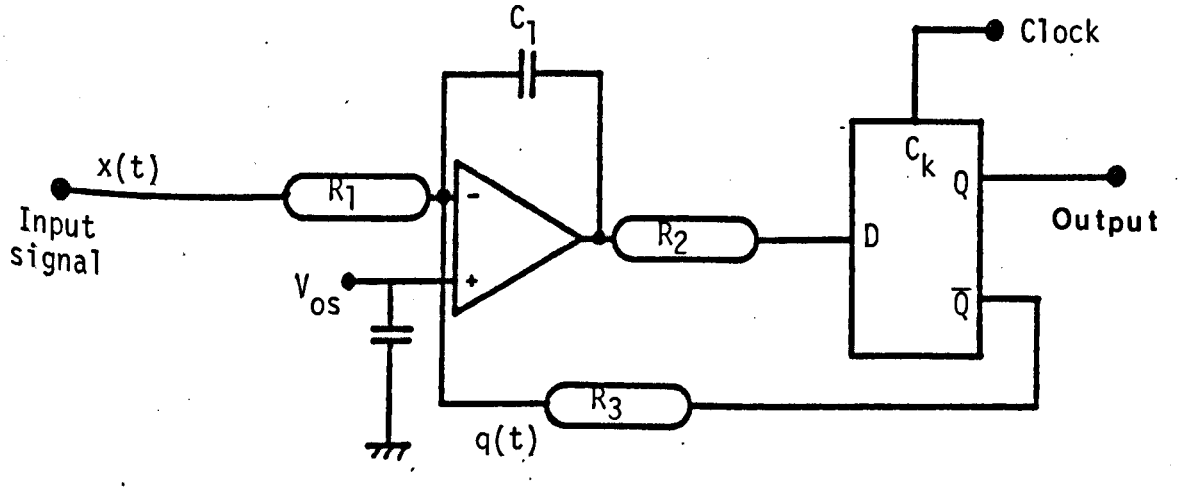


Figure 2.3 Circuit of analogue d.s.m.

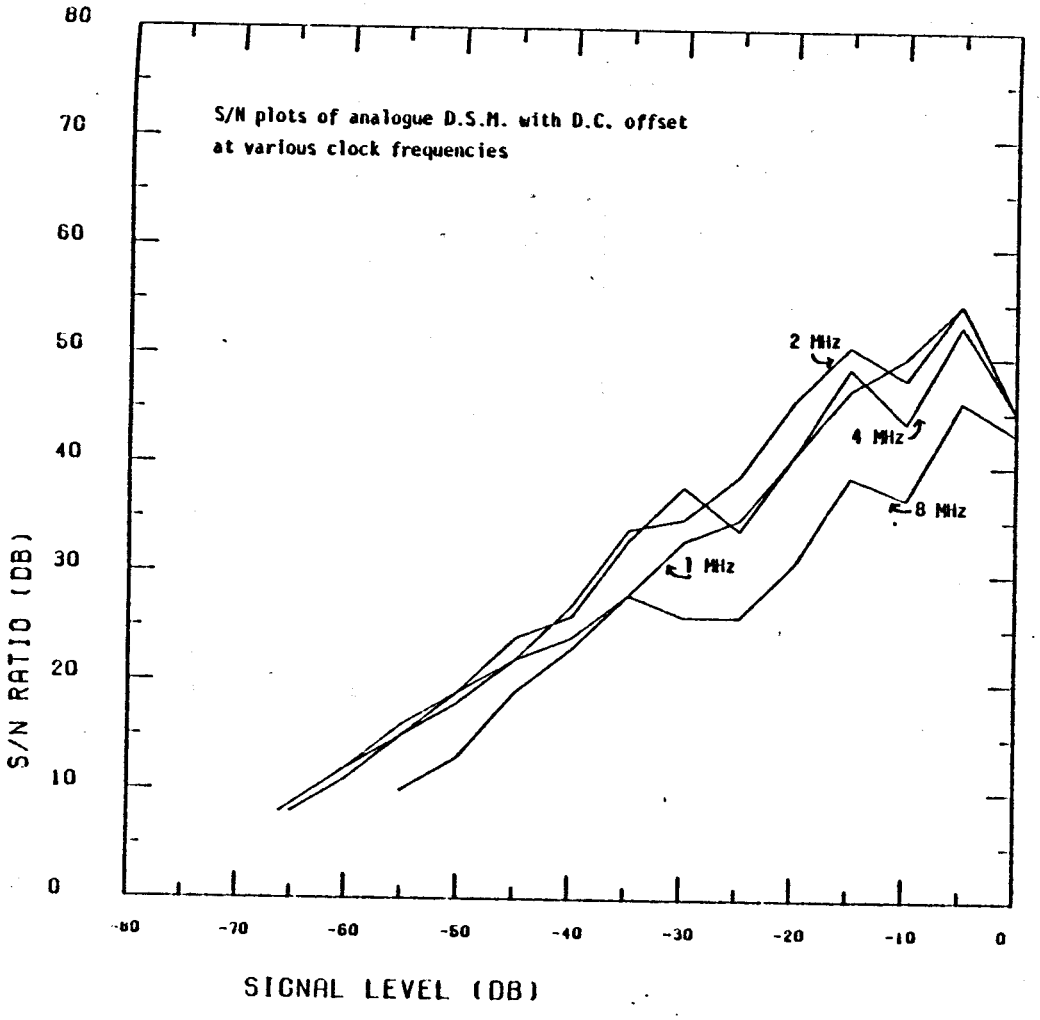


Figure 2.5

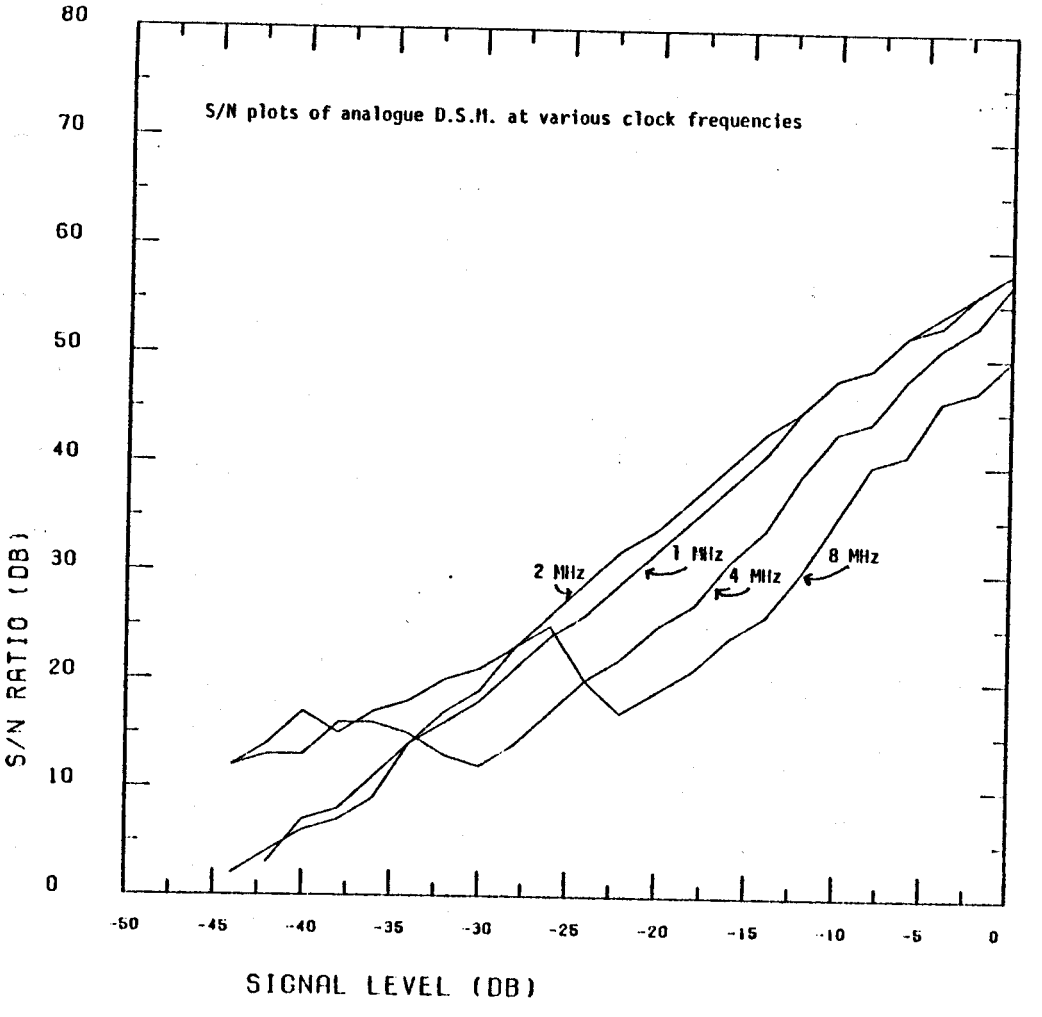


Figure 2.4

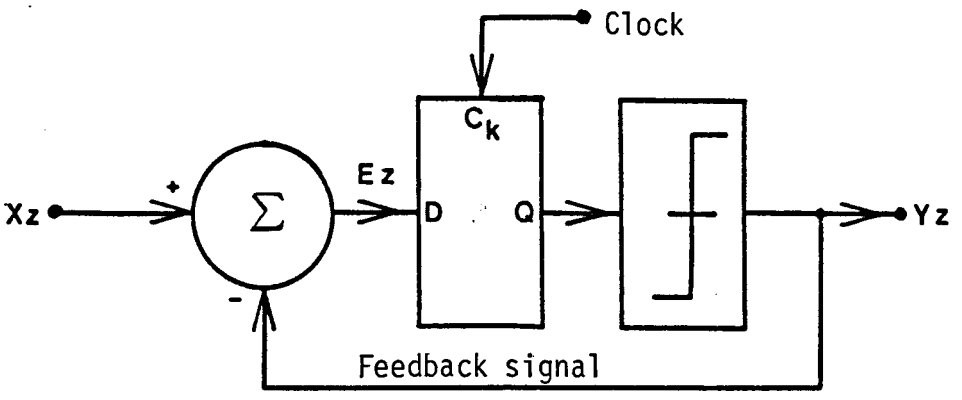


Figure 2.6 Functional diagram of a d.d.s.m.

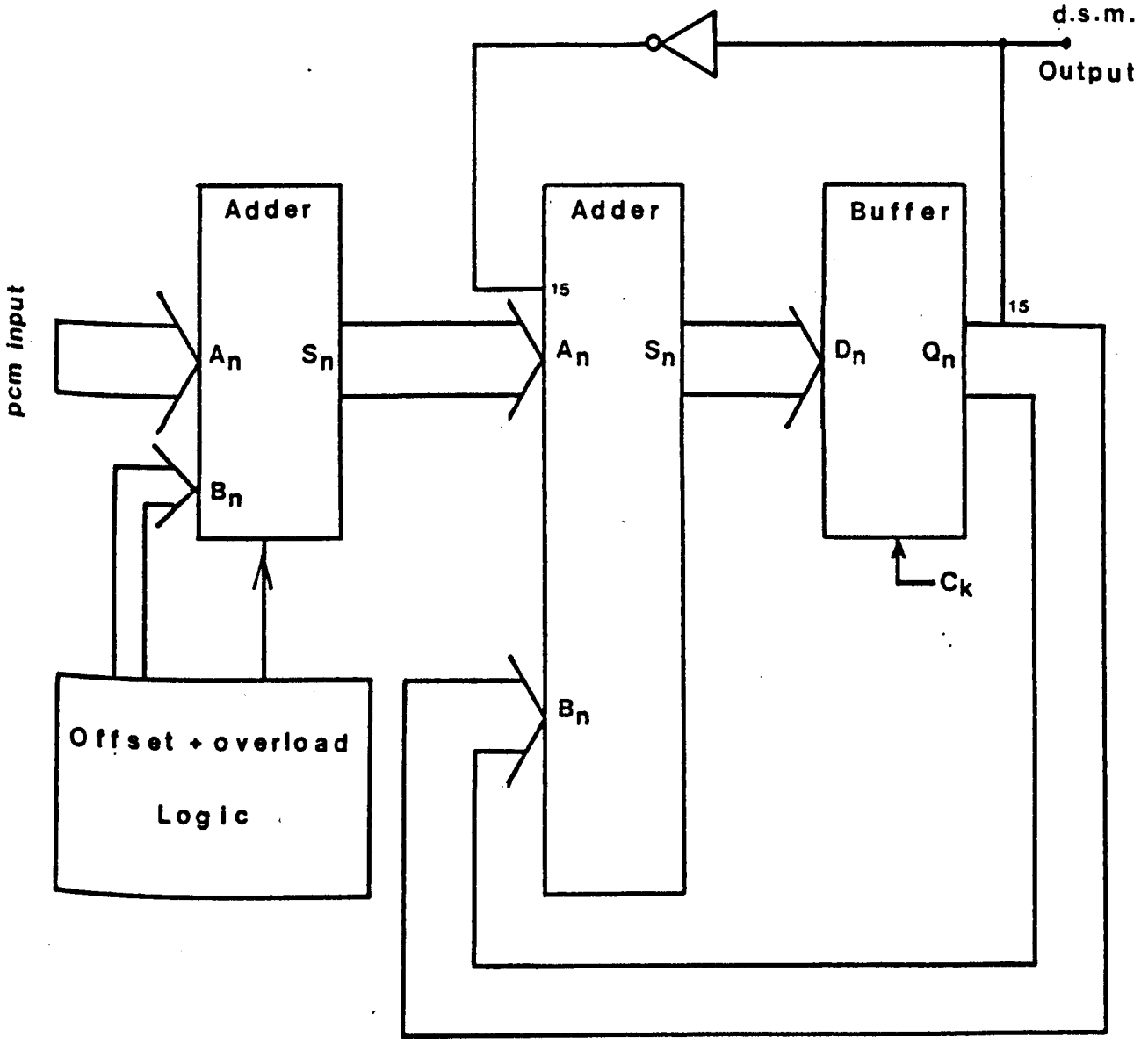


Figure 2.7 Circuit of a digital d.s.m.

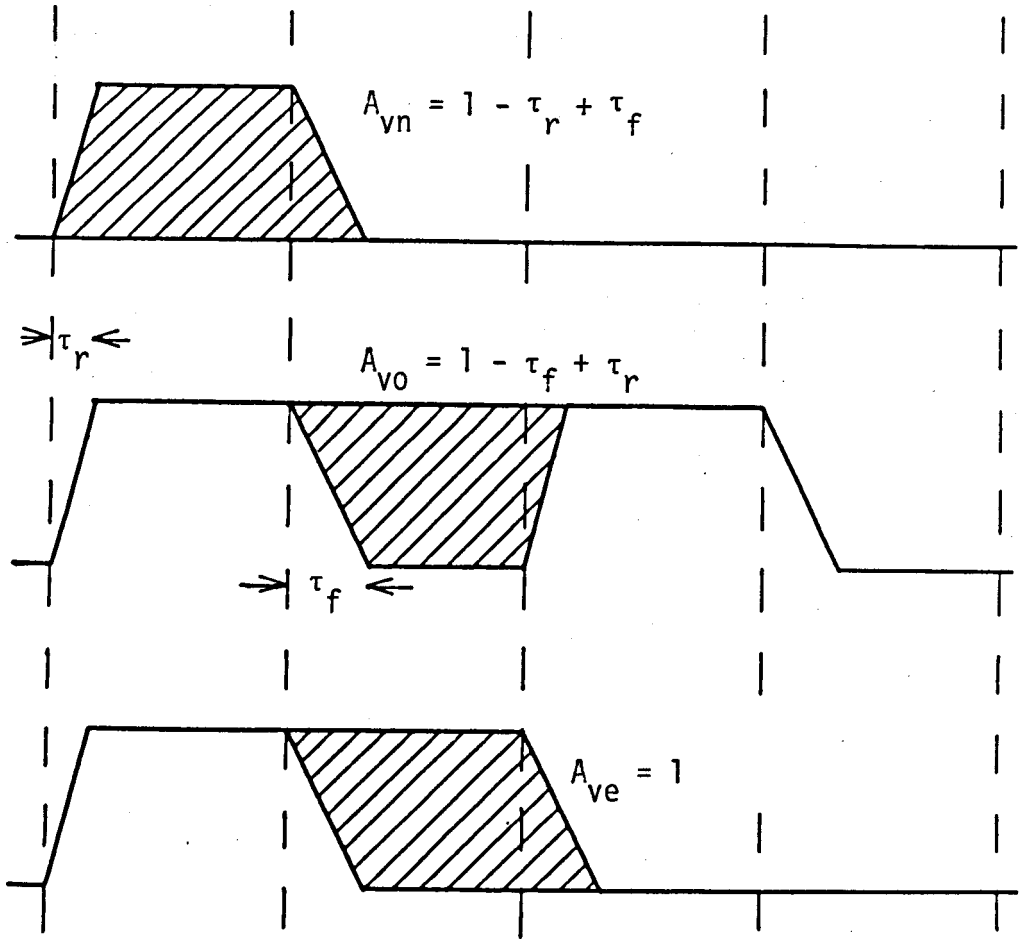


Fig. 2.8a

Fig. 2.8b

Fig. 2.8c

Figure 2.8 The increases in area associated with the three possible positions of an extra pulse in a pulse pattern.

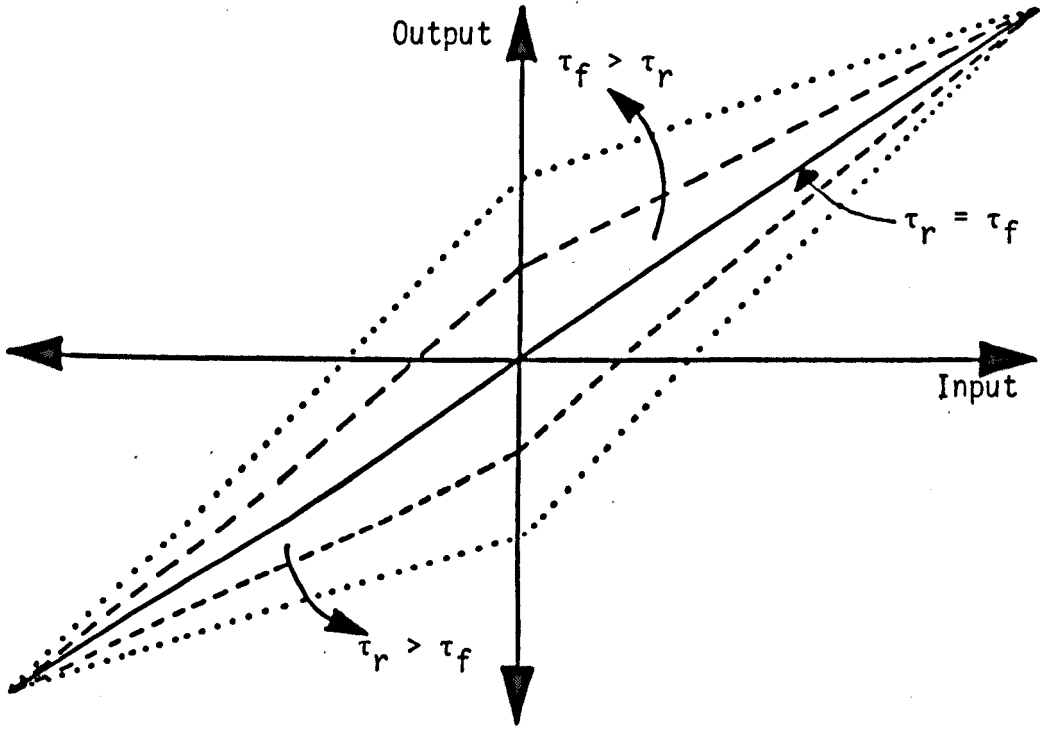


Figure 2.9 A copy of a computer simulation of the D.C. transfer characteristics produced by different values of τ_r, τ_f in a D.S.M. output pulse pattern.

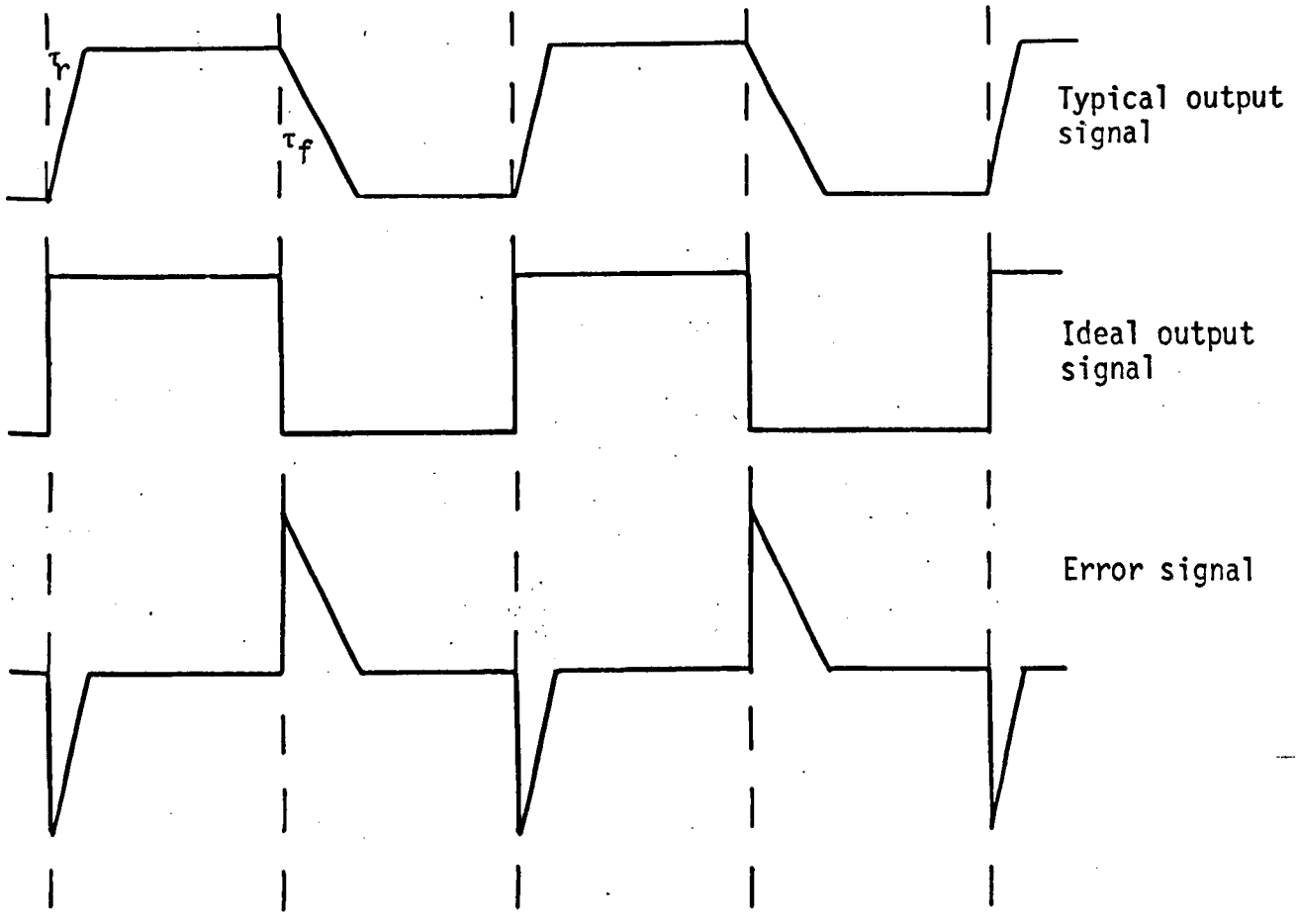


Figure 2.10 Diagrams showing a typical output pulse pattern and its constituent components.

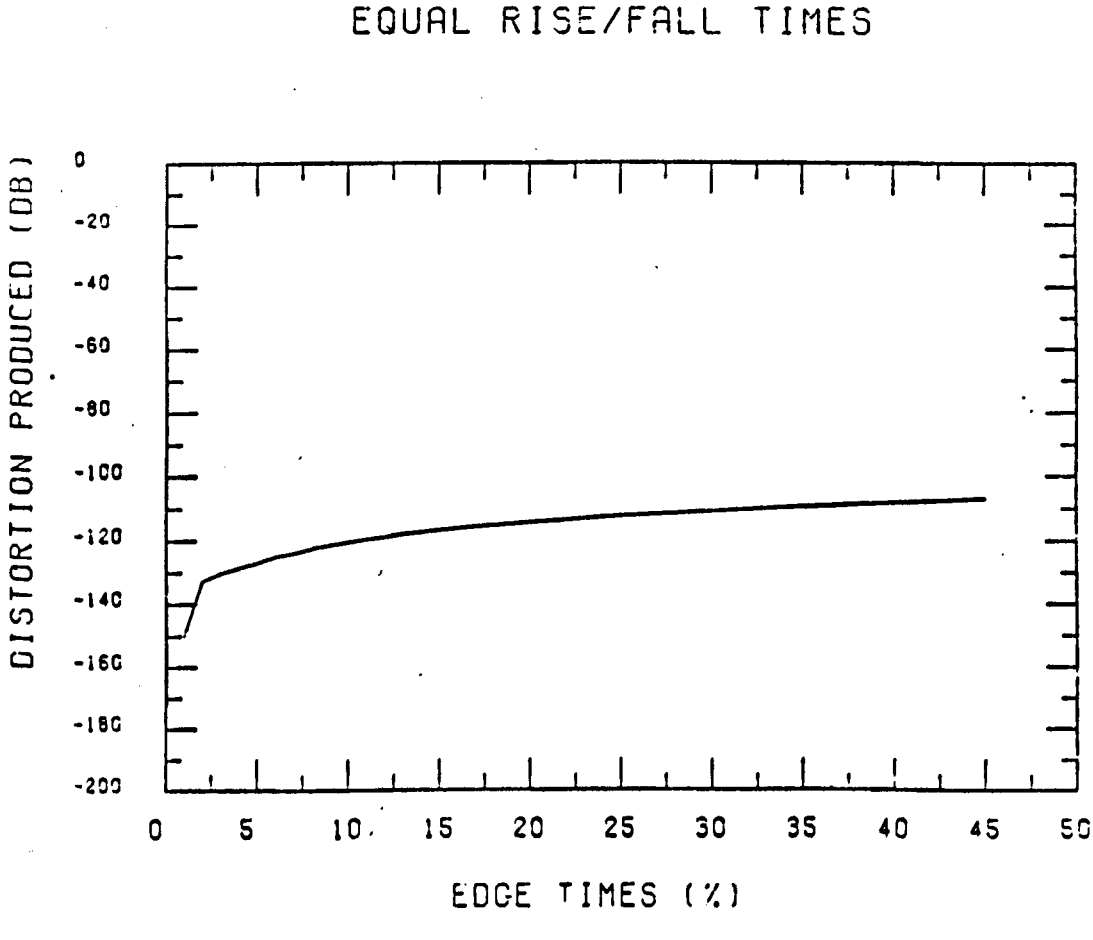


Figure 2.11 The simulated levels of distortion produced by a D.S.M. with equal edges on the output pulse pattern.

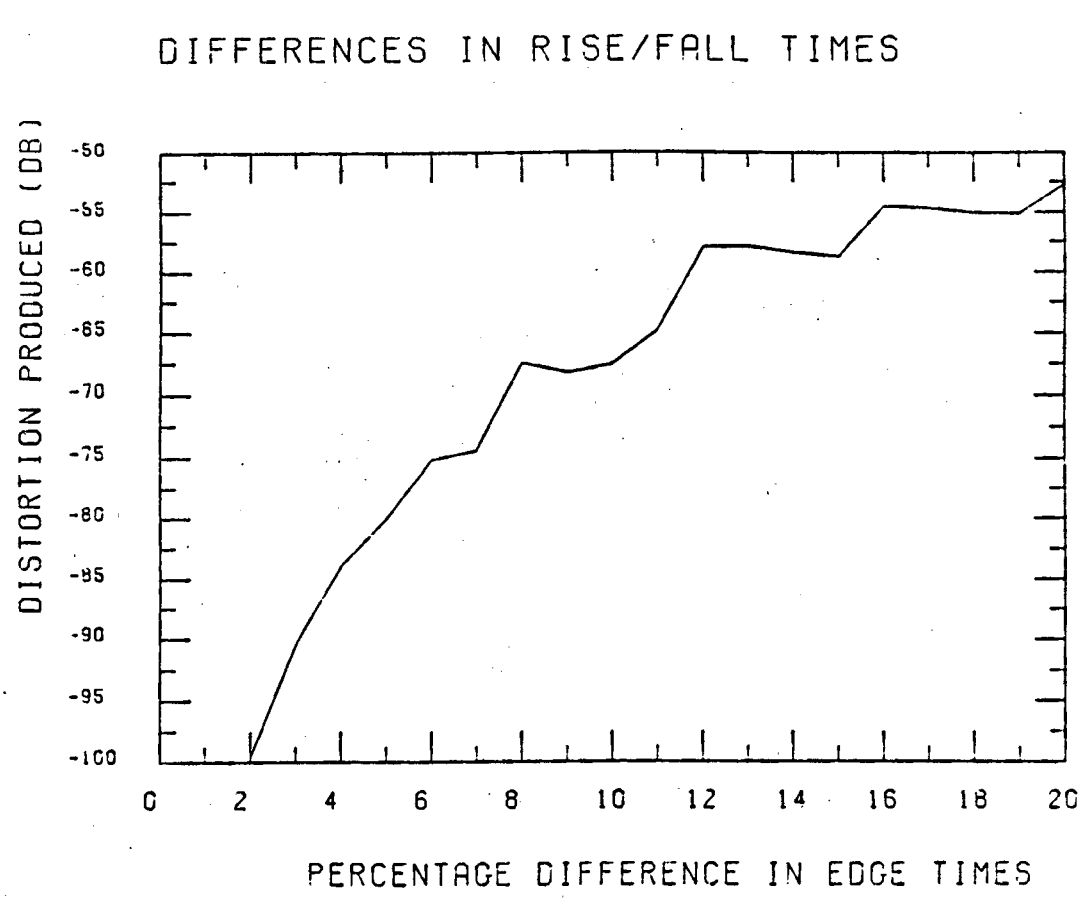


Figure 2.12a The simulated levels of distortion produced by a D.S.M. with unequal edges on the output pulse pattern.

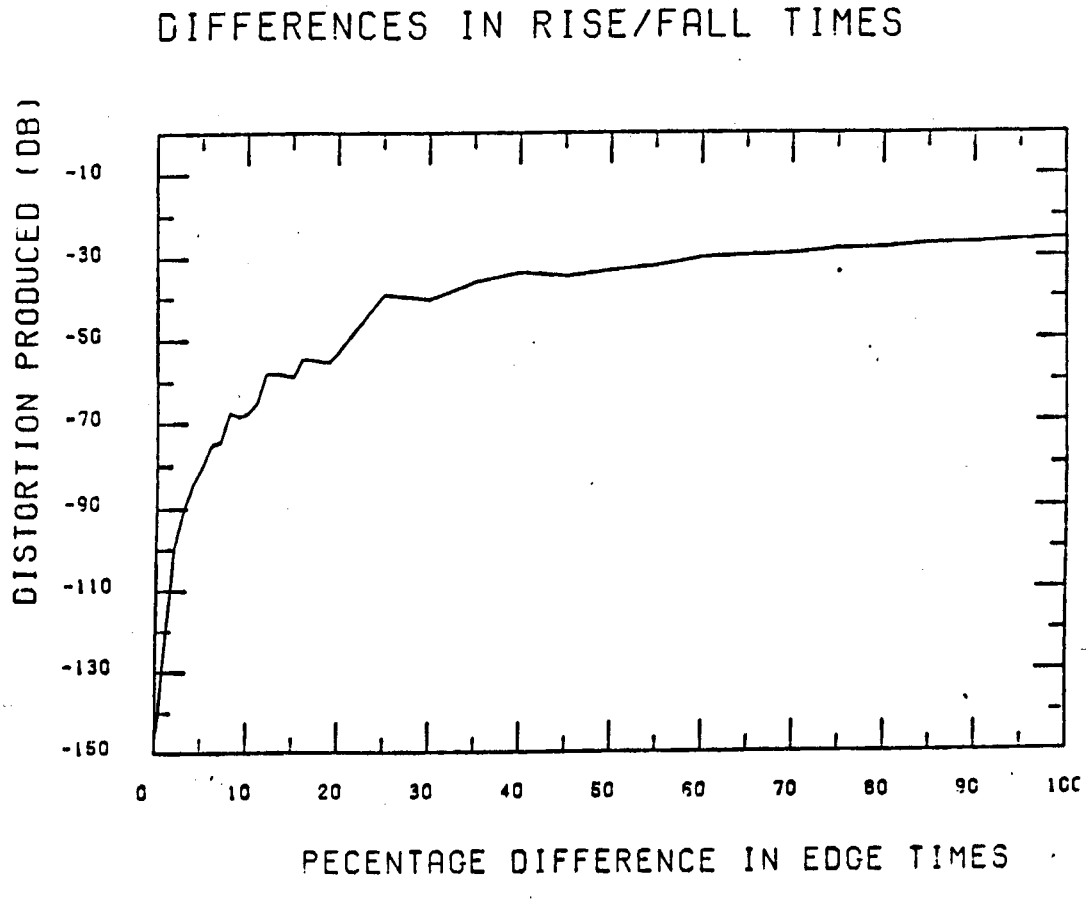


Figure 2.12b An extension of the scale used in Figure 2.12a.

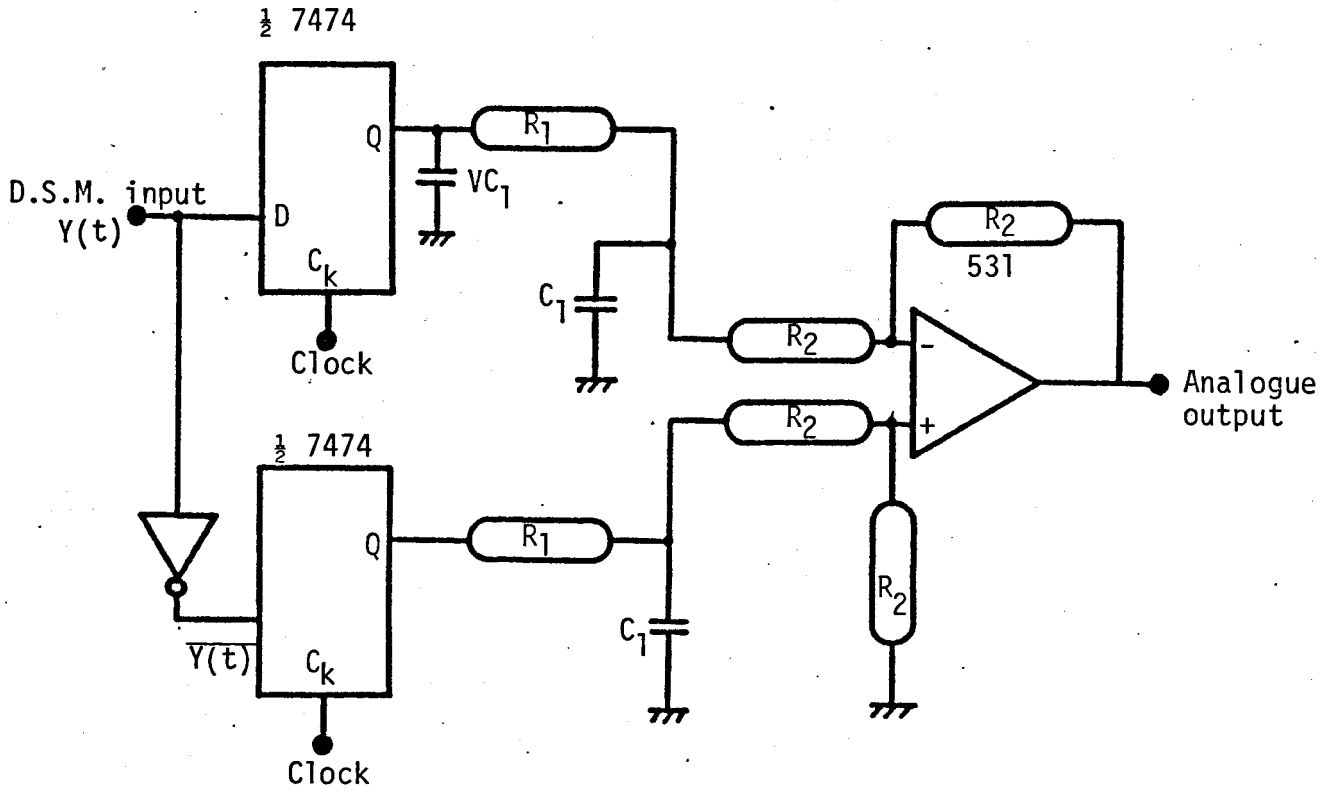


Figure 2.13 The differential output circuit, used to correct for unequal rise and fall times in the D.S.M. output.

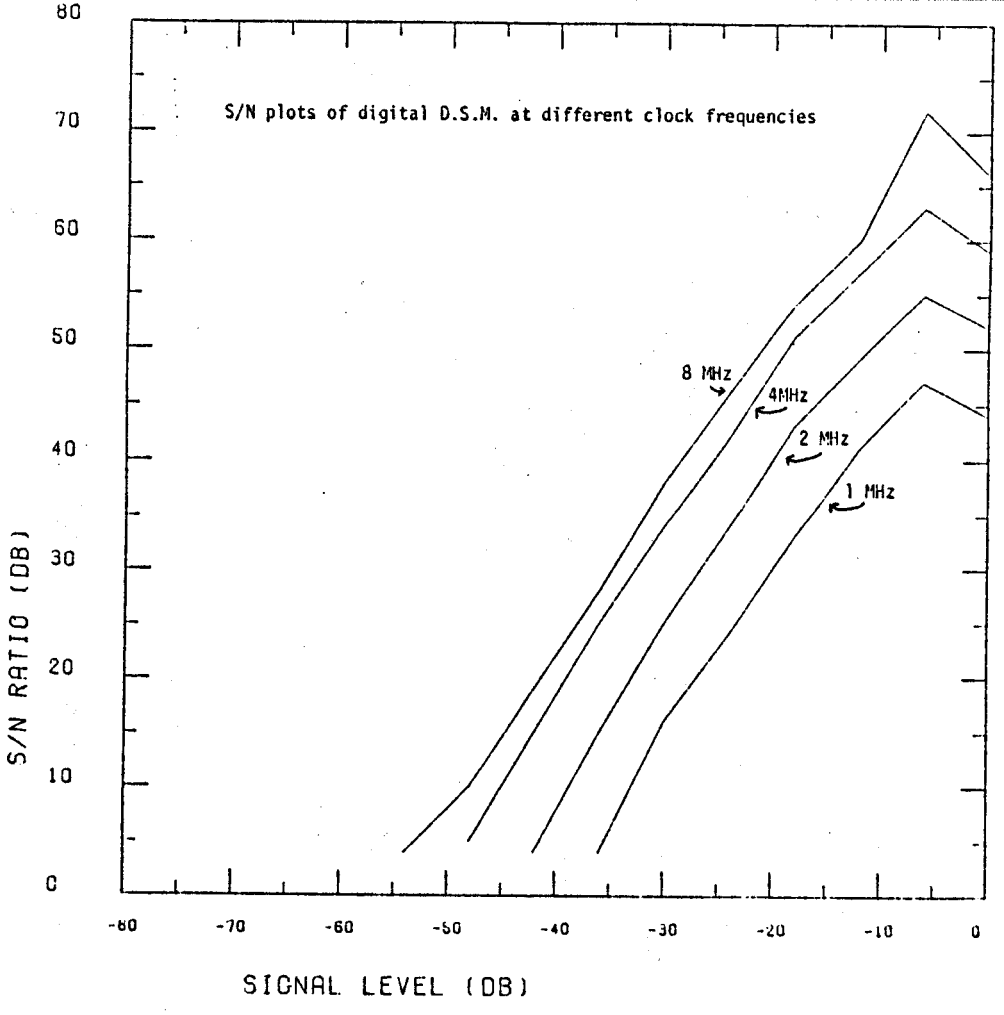
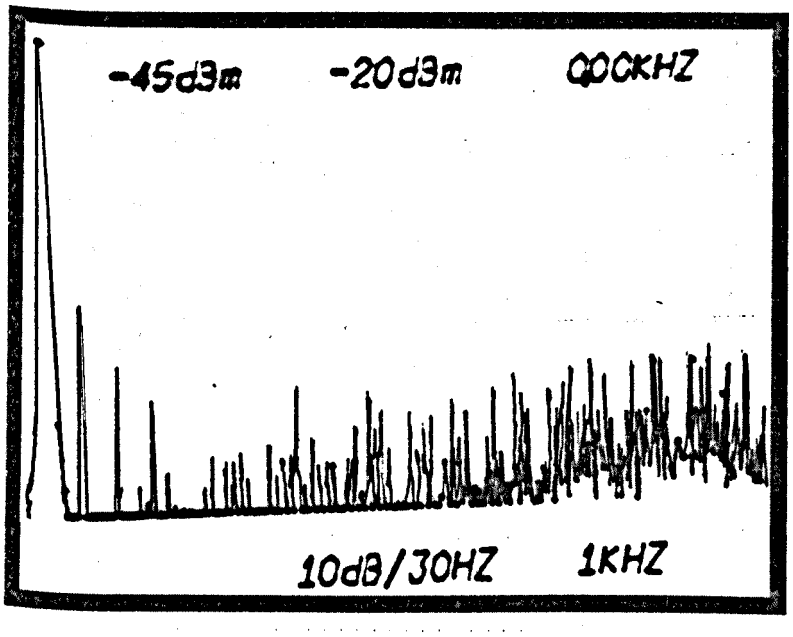


Figure 2.14 Performance of the digital d.s.m. over a range of clock frequencies.



Vert. scale
10 dB/0.8 cm

Horiz. scale
1 KHz/0.8 cm

Bandwidth
30 Hz

Fundamental	=	- 6 dB
2nd Harmonic	=	-84 dB
3rd Harmonic	=	-90 dB
4th Harmonic	=	-
Idle channel noise	=	-86 dB

Figure 2.15 Harmonic spectrum of the D.S.M. at a 4 MHz clock frequency.

Figure 2.16a P.D.F. of a sine wave

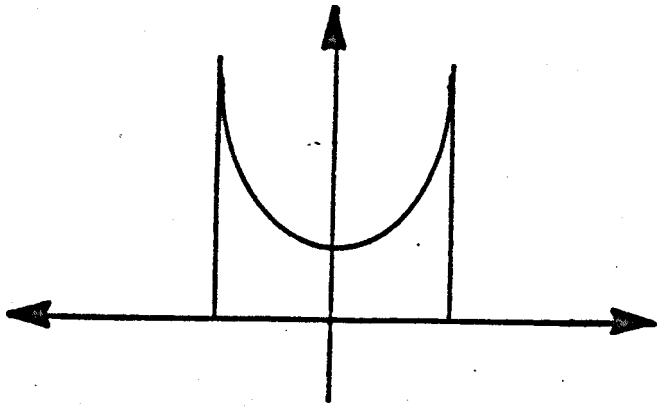


Figure 2.16b Addition of a D.C. offset

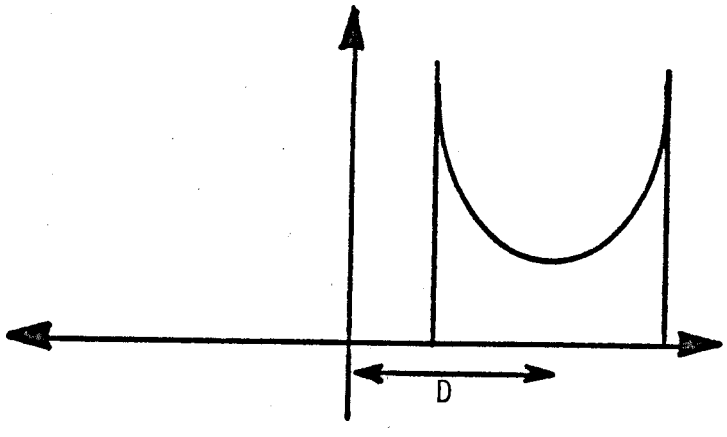


Figure 2.16c P.D.F. of a large sine wave

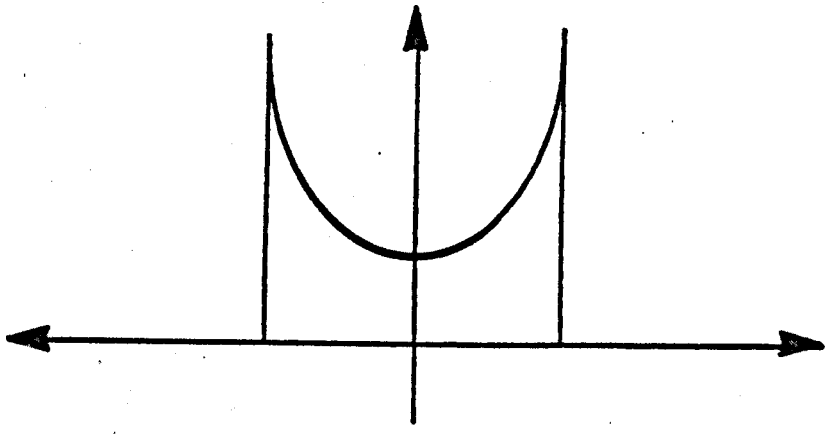


Figure 2.16d Addition of an offset equal to peak signal

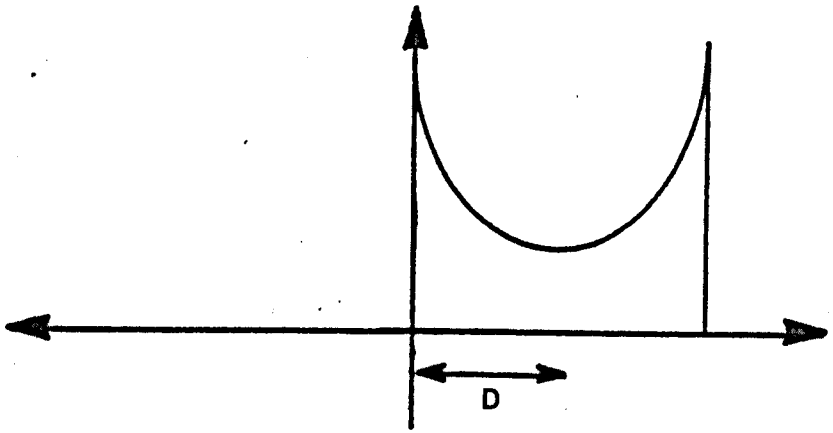


Figure 2.16 The change in P.D.F. of the input signal applied to the D.S.M. when different D.C. offsets are added.

Figure 2.17 The effect on the modulator's spectrum when different offsets are applied to the input signal.

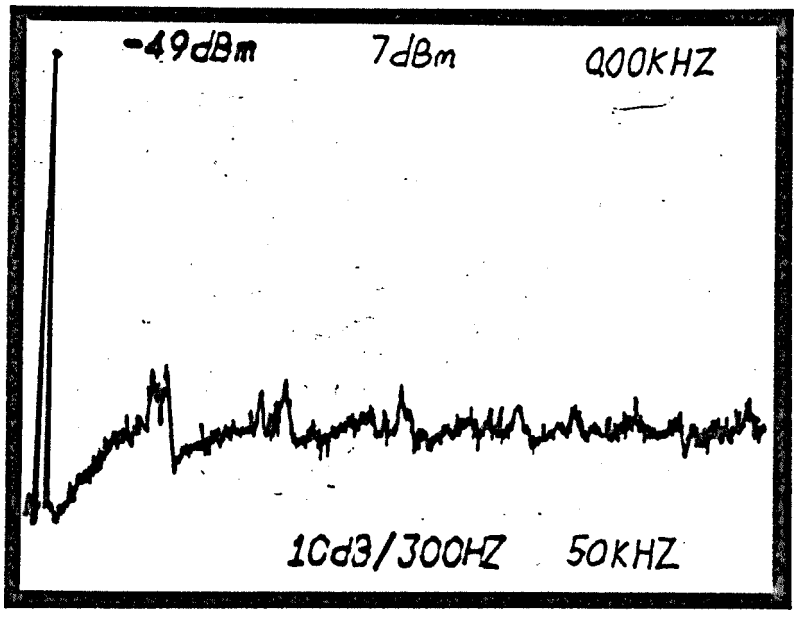


Figure 2.17a
Noise spectrum produced by a d.s.m.

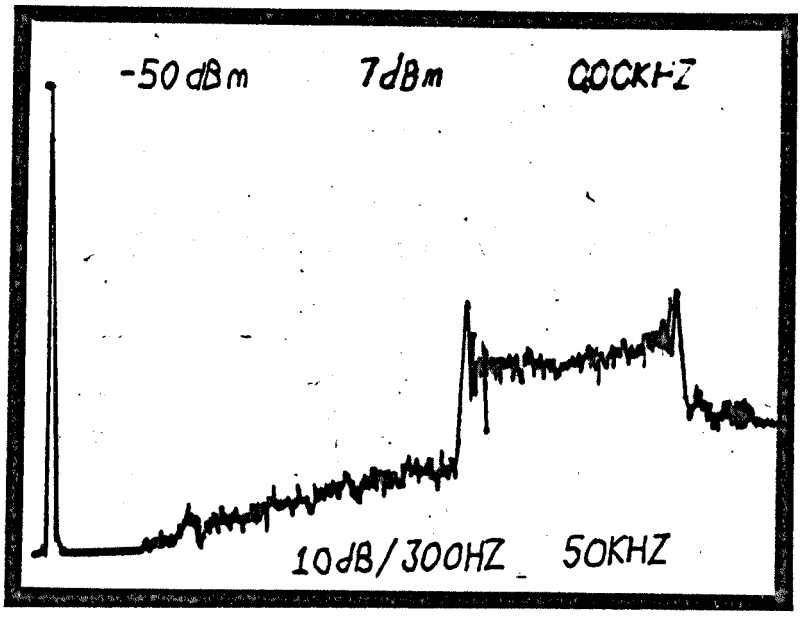


Figure 2.17b
The effect of adding a D.C. offset.

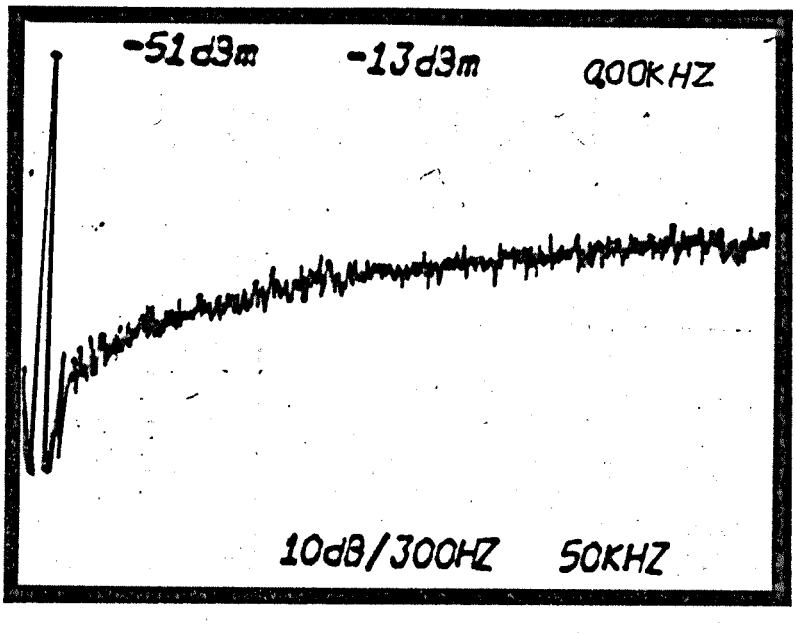


Figure 2.17c
The increase in noise when the input signal equals the applied offset.

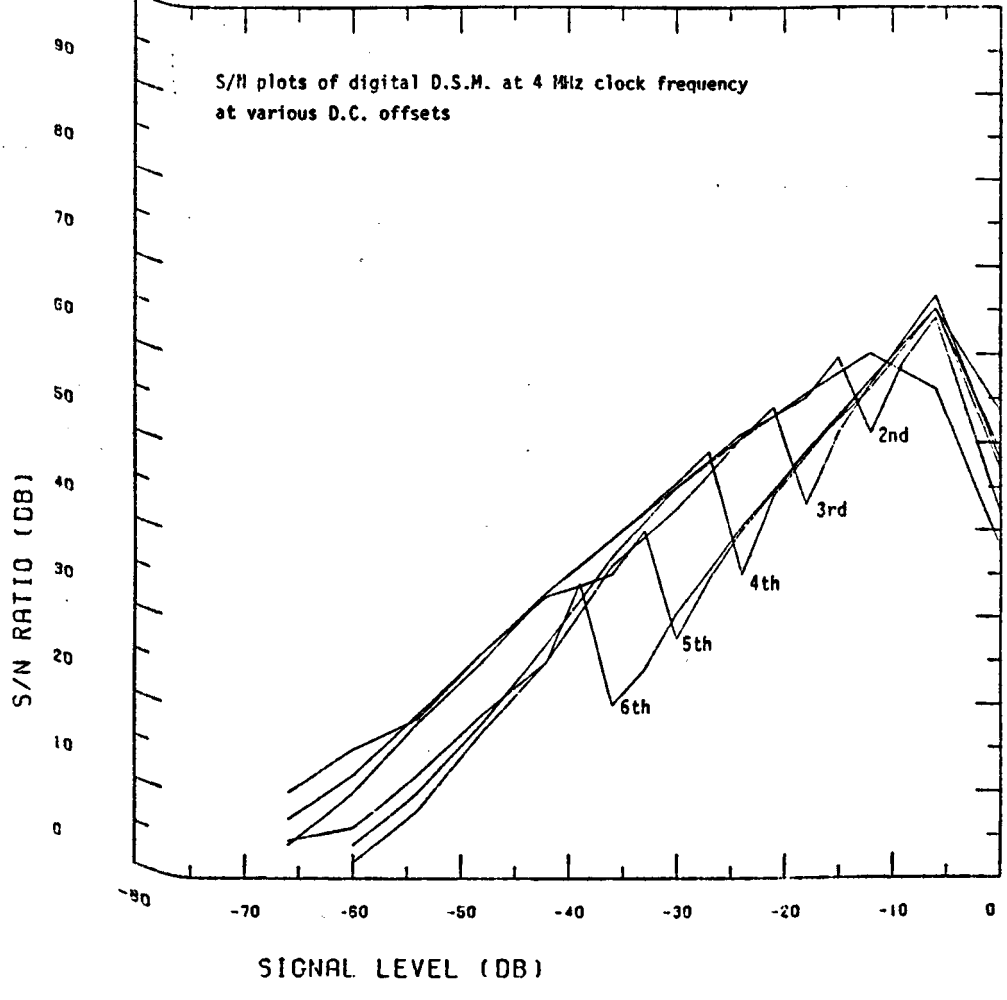
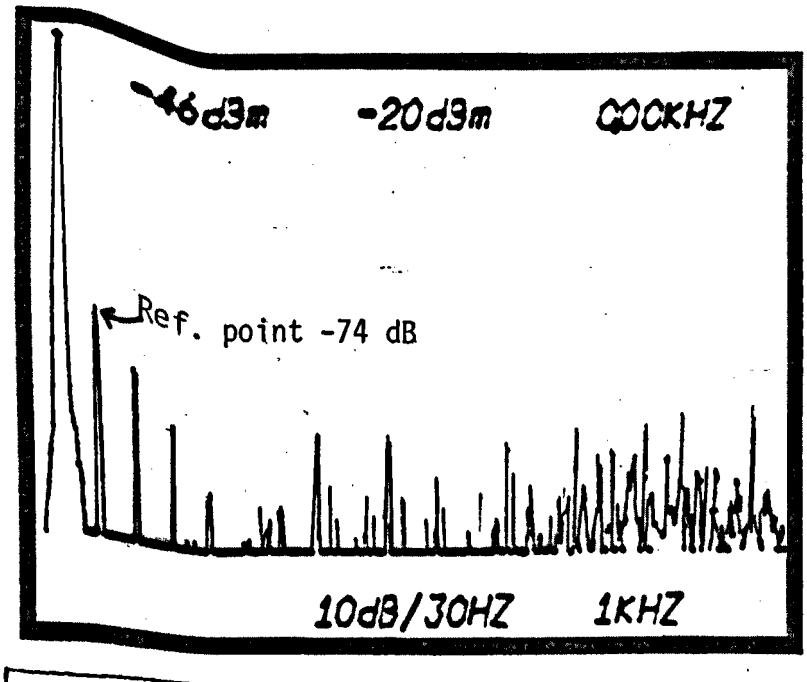


Figure 2.18a-g The variation in S/N of a D.S.M. clocked at 4 MHz when different D.C. offsets are applied.



Vert. scale
10 dB/0.8 cm

Horiz. scale
1 kHZ/0.8 cm

Bandwidth
30 Hz

Fundamental	=	- 6 dB
2nd harmonic	=	-78 dB
3rd harmonic	=	-86 dB
4th harmonic	=	-91 dB
Idle channel	=	-87 dB

Figure 2.18h The harmonic spectrum of the modulator when the offset is added to the fourth bit.

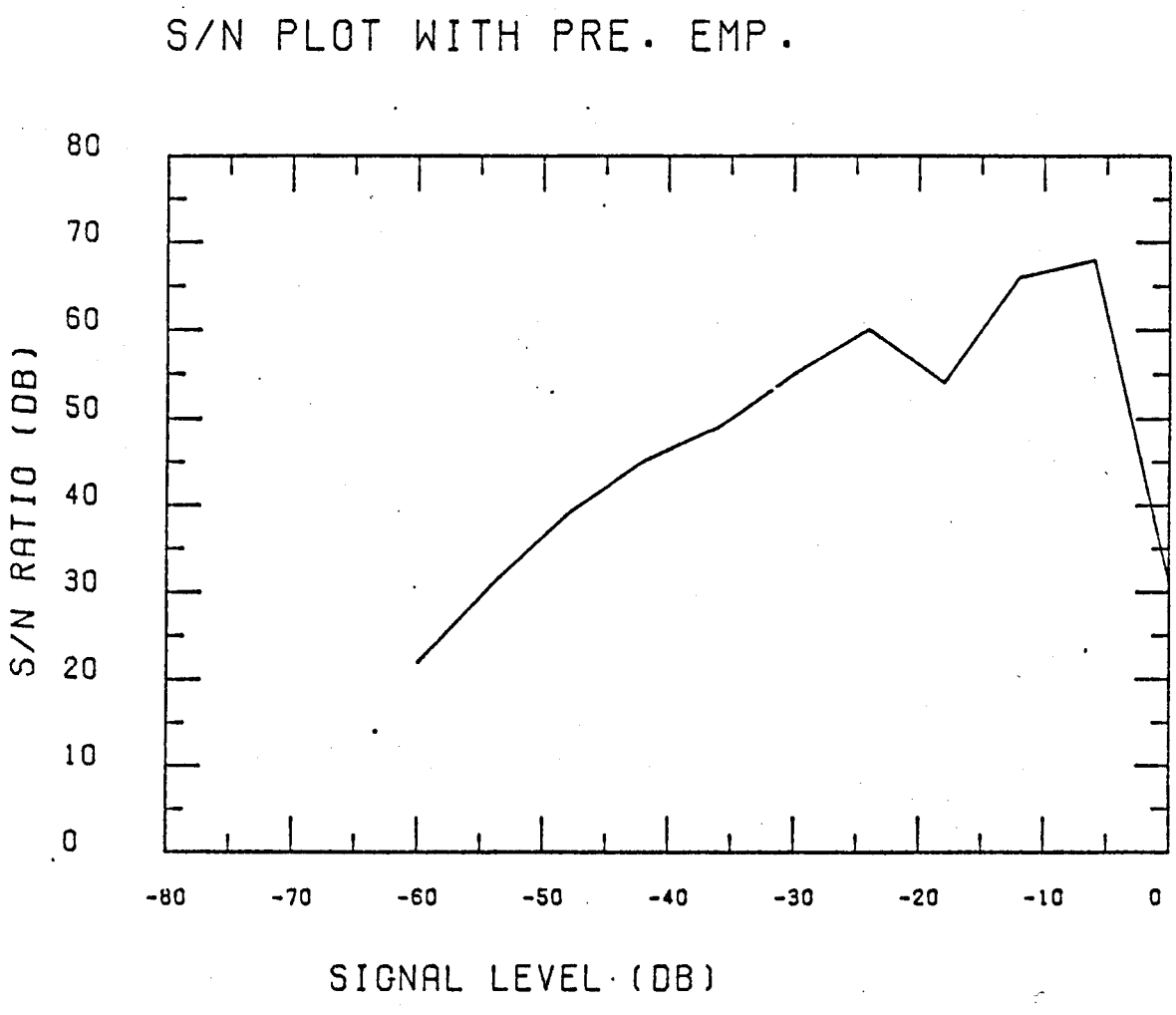


Figure 2.19a Results of using de-emphasis on the modulator's S/N.

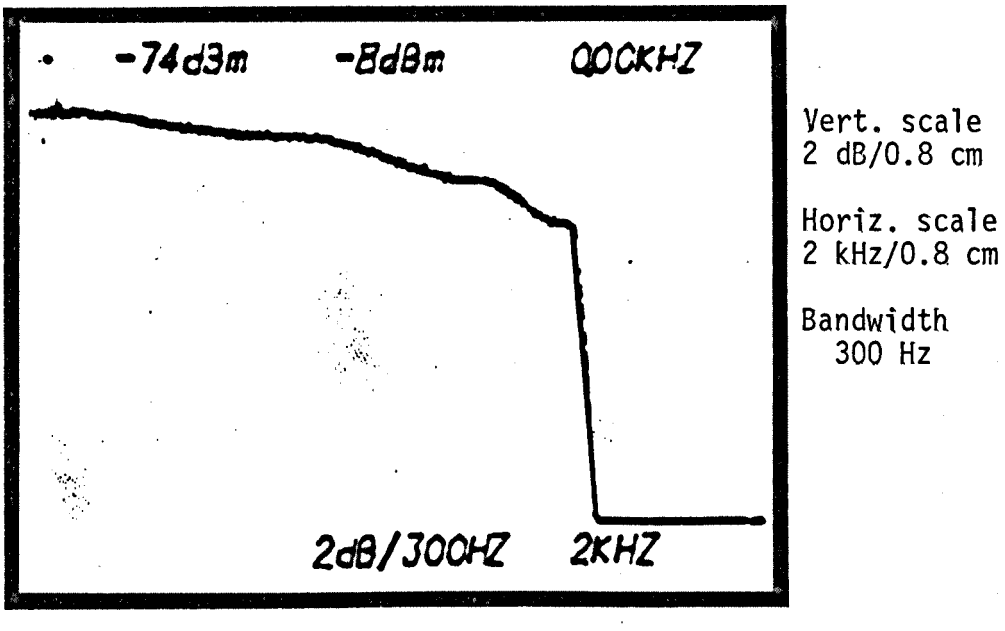


Figure 2.19b The coder's frequency response indicating drop due to the $\frac{\sin x}{x}$ function.

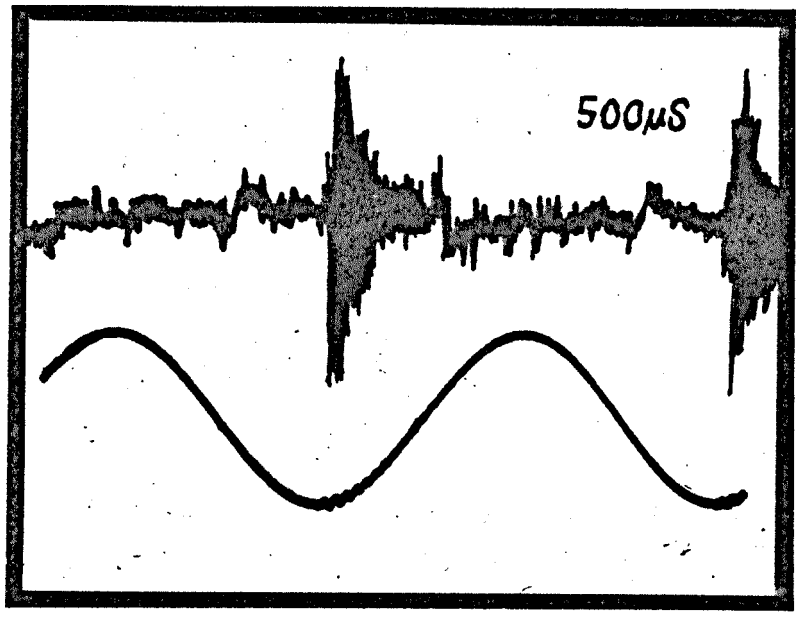


Figure 2.20 Burst of noise produced by modulator when the input signal equals applied offset.

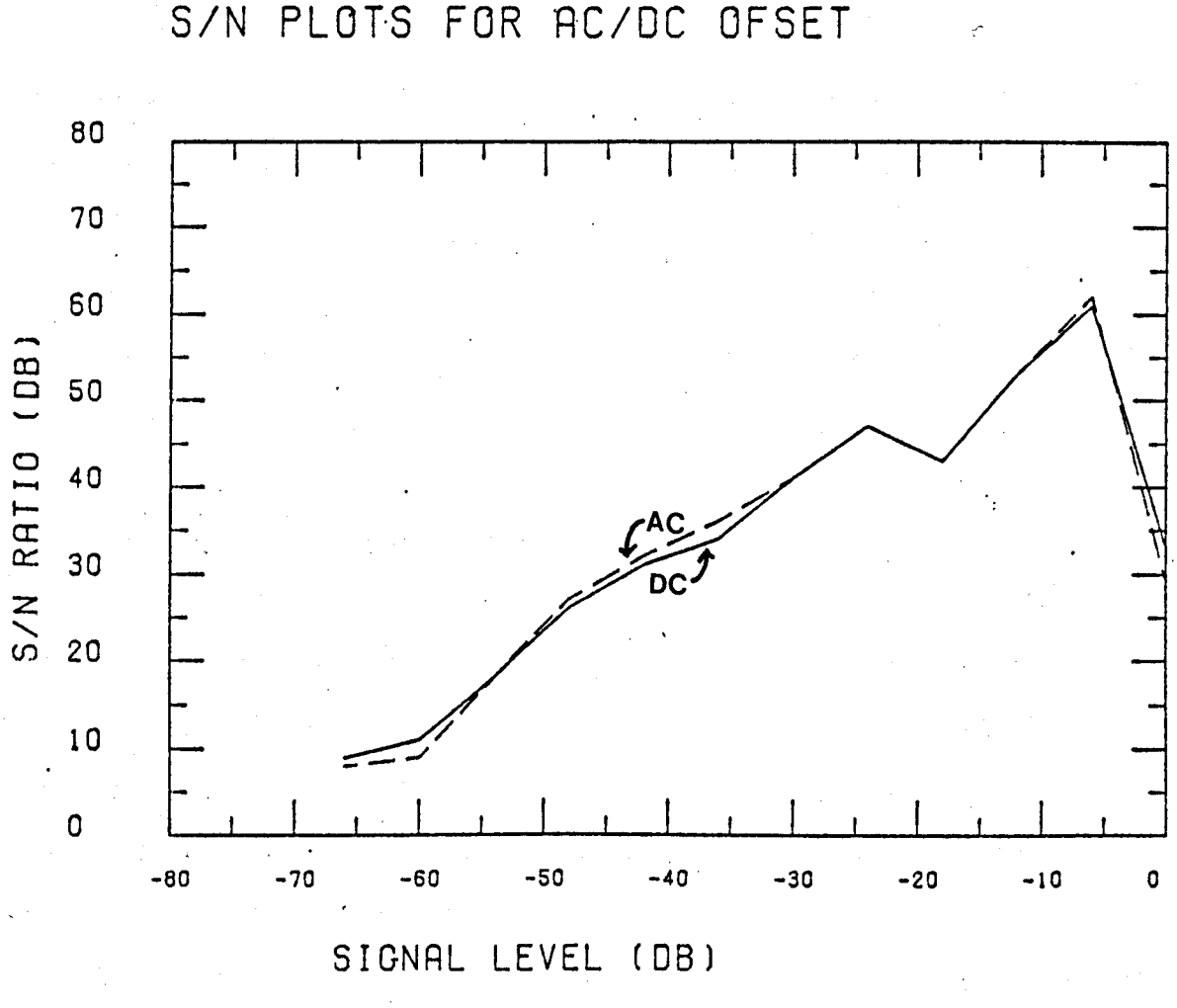


Figure 2.21 Comparison of S/N ratios of a modulator when DC and AC offsets are applied.

CHAPTER 3

ERROR CORRECTION TECHNIQUES

In Chapter 2 the idea of using a code-converter to convert a P.C.M. signal into an oversampled one-bit signal was introduced. A d.s.m. was described, tested and shown to be suitable for this application. Delta sigma modulation was used because it produced a code which could be simply decoded into an analogue voltage. This type of system produced a digital to analogue (D/A) converter with few analogue components at the expense of providing additional digital hardware for code conversion.

A single d.s.m. is unsuitable for high quality D/A conversion at practically useable clock rates. However, the basic d.s.m. contains little digital hardware and so can be manufactured very cheaply. It is therefore economically feasible to investigate techniques of improving their performance at the expense of providing additional digital circuitry. One technique, described in this chapter, separates the error produced by a d.d.s.m. from the wanted signal to provide an error-free output.

3.1.1 Error Feed-forward Correction

In 1924 H.S. Black (Ref. 3.1) proposed a method of improving an amplifier's linearity by detecting any error produced by the amplifier and feeding it forward to the output in such a manner so as to cancel its effect. This arrangement, shown in Figure 3.1, was regarded as a curiosity at the time, however, recent work (Refs. 3.2, 3.3) suggests that the usefulness of the original concept was underestimated.

The original feed-forward amplifier operates as follows:- the output of the main amplifier (A) is attenuated and subtracted from the input signal. If the gain and phase delay introduced by the main amplifier is

exactly compensated by the attenuator (N), the summed output (e) will consist of the extraneous noise (error) components produced by the main amplifier. The error signal (e) is then amplified by the second amplifier (B) and subtracted from the output of the main amplifier. Thus the imperfections at the main amplifier's output are cancelled and do not appear in the final output. Since the second amplifier only operates over a small dynamic range, it can be made very linear. This technique results in a highly linear system, but entails careful matching of phase and amplifier gains to ensure correct operation.

This error feed-forward technique can be applied to digital delta sigma modulators to improve their performance. The way in which this is done is described in section 3.2.1. However, before the application of the technique can be discussed in detail it is necessary to show how p.c.m. can be re-constituted from delta-sigma code. It will be seen later that this is a necessary process in producing the feed-forward error signal.

3.1.2 Conversion of D.S.M. to P.C.M.

To use the error feed forward system to improve a d.d.s.m. it is necessary to obtain the single bit D.S.M. output in the same form as the original P.C.M. input. This requires code converting the D.S.M. code back into P.C.M.

Recent work by Goodman (Ref. 3.4) has shown how digitally filtering a D.S.M. data stream can produce P.C.M. Other experimenters (Ref. 3.5 and 3.6) have used analogue d.s.m. and used digital filters to produce analogue to digital converters at low cost.

As a D.S.M. code is oversampled it is desirable to reduce the sampling rate when the code is filtered, to the same rate as the required P.C.M. output. The requirements of a filter to convert D.S.M. to P.C.M. can be summarized as follows:-

i. The D.S.M. output needs low pass filtering to remove all

unwanted out-of-band noise.

ii. The resulting oversampled output P.C.M. from the filter needs subsampling to the appropriate Nyquist Rate.

To appreciate the need to filter a signal before subsampling and the consequential increase in the number of bits describing the original signal, consider an oversampled signal with a sample rate f_m. Assume that subsampling to a new rate f_s every n^{th} sample is taken, and intermediate samples discarded, where n is determined from:-

$$n = \frac{f_m}{f_s} \qquad 3.1$$

The re-sampling action described would cause the noise in the band between $f_{s/2}$ to $f_{m/2}$ to be aliased into the message band ($f_{s/2}$). This would considerably reduce the in-band signal-to-noise. If an ideal low-pass filter was used to filter the oversampled signal with a frequency response described by:-

$$H(z) = 1, \quad f \leq f_{s/2}$$

$$H(z) = 0, \quad f > f_{s/2}$$

When this signal is subsampled no additional noise would be aliased into the message band. As a large number of samples have been discarded, and in the latter case, no increase in noise has occurred, the accuracy of the remaining samples needs to be adequate to ensure the fidelity of the original signal. If the original signal was a single bit, the final signal will be represented by multi-bit samples.

To keep the overall complexity of the proposed noise-shaping coder simple the filter required to convert D.S.M. to P.C.M. must be simple. So the structure of the filter must be chosen to reduce the amount of multiplication required to a minimum. For a filter to be used in this application

it must meet the following specifications;-

i. Have a linear phase response (so that the filter delay can be compensated by a simple shift register delay in the other path to the subtractor producing the error signal).

ii. Produce minimal in-band frequency attentuation.

iii. Reduce the out of band noise to a minimum

iv. Be as simple as possible.

The type of filter used in similar applications (Refs. 3.5, 3.6) meets these criteria and is now discussed.

Any filter which has a symmetrical impulse response about t=0 has a zero phase delay at all frequencies. A digital filter whose impulse response begins before t=0 is not physically realisable, however, such a filter can be converted into a realisable one by shifting the impulse response along in time so that it begins at t=0. This produces a filter with a purely real frequency response and linear phase characteristic.

A general non-recursive filter with m coefficients will have the transfer function, described in the z-domain as;-

$$H(z) = A_0 + A_1 z^{-1} + A_2 z^{-2} - - - - A(m-1) z^{-(m-1)} \qquad 3.4$$

The implementation of this filter can be greatly simplified if all the coefficients are equal. It can then be constructed in the recursive form. The recursive form of H(z) is:-

$$H(z) = \frac{1-z^{-m}}{1-z^{-1}} \qquad 3.5$$

Implementation of this filter is particularly simple if the equal coefficients are made unity. The frequency response of such a filter (H(jf)) is given by;-

$$H(jf) = \frac{1 - e^{-jm2\pi fT}}{1 - e^{-j2\pi fT}} \qquad 3.6$$

Provided that $f \ll \frac{1}{T}$ this approximates to a sin x/x response, shown in Figure 3.2, and described by:-

$$H(f) = \frac{\mathrm{Sin}(m\pi fT)}{(m\pi fT)} \qquad 3.7$$

This type of filter was used by the B.B.C. in experimenting on the use of D.M. in A/D conversion (Ref. 3.6).

An increase in the out of band attenuation can be obtained by cascading two of these filters. This has the same effect as using one filter with a triangular set of weighting coefficients (Ref. 3.7). More generally, cascading a filter of m uniform weighting coefficients with a similar filter of n uniform weighting coefficients gives the following frequency response, given by:-

$$H(f) = \frac{\mathrm{Sin}(m\pi fT)}{(m\pi fT)} \cdot \frac{\mathrm{Sin}(n\pi fT)}{(n\pi fT)} \qquad 3.8$$

if m = n then this simplifies to:-

$$H(f) = \frac{\mathrm{Sin}^2(m\pi fT)}{(m\pi fT)^2} \qquad 3.9$$

This is shown in Figure 3.2b. Such a filter is particularly simple to construct in the recursive form. The recurrence formula is:-

$$y(n) = -y(n-2) + 2y(n-1) + x(n-2m) - 2x(n-m) + x(n) \qquad 3.10$$

Only integer multiplication by 2 and -1 is required, and this can be accomplished without multiplication hardware, using shift and add arithmetic.

3.2.1 Feedforward Techniques in Digital to Analogue Conversion

The error feed-forward system outlined in section 4.1.1 can be employed in a D/A converter using d.d.s.m. This is possible since the previous section showed how the output of a digital delta sigma modulator can be reconstituted as P.C.M. This can then be compared with the original P.C.M. input and an error signal produced, which can then be fed forward

to provide an error free output. This chapter describes new techniques for separating the error produced by a basic d.d.s.m. from the required output signal and its subsequent use to produce an error-free D/A converter.

The output of the d.d.s.m. can be considered as containing two components:-

i) The input signal

ii) An error signal

This is shown in the illustration of the proposed error-feed forward system, Figure 3.3.

In this system the output of the linear d.d.s.m. is $X(z) + E(z)$, where $X(z)$ is the applied P.C.M. input signal, and $E(z)$ is the error noise produced by the modulator (d.d.s.m. 1). This output is filtered by the linear phase filter ($H(z)$) and subtracted from the input signal delayed by z^{-n} (to compensate for the delay introduced by the filter). The filter response can be approximated by:-

$$H(z) = 1, \quad f \leq f_c \qquad f_c = \text{max signal frequency}$$
$$H(z) = 0, \quad f > f_c$$

The resulting signal is then scaled by a constant factor (k) and applied to the second d.d.s.m. (d.d.s.m. 2). The input to this second modulator consists of the in-band noise ($E(z)$) produced by the first modulator. When scaled by k this can be expressed as:-

$$E'(z) = k|X(z)\, z^{-n} - (X(z) + E(z)).H(z)|$$
$$\simeq k\, E(z)\, .\, H(z) \qquad 3.11$$

This in turn is encoded by the second modulator, re-scaled by $1/k$ and subtracted from the output of the first modulator. If the second modulator itself produces noise ($F(z)$) and the output filter has a low-pass response ($M(z)$) similar to ($H(z)$), the overall output of the system will be given by:-

$$Y(z) = \left| (X(z) + E(z) \quad , \quad z^{-n} - \frac{(E'(z) + F(z))}{k} \right| * M(z) \qquad 3.12$$

which for the message band simplifies to:-

$$Y(z) = X(z) + F(z)/k$$

If E(z) and F(z) are of similar magnitude the noise produced by the system will be reduced by k.

3.2.2 Theoretical Evaluation of k

Equation 3.13 shows how the error feed-forward technique can be used to improve the noise performance of a d.d.s.m. The improvement obtained depends on the value of k selected, which in turn depends on:-

i. k should be as large as possible to reduce the noise produced by the second encoder.

ii. k should not be so large as to cause the second encoder to be overloaded.

To select the optimum value of k a knowledge of the statistics of the noise applied to the second d.d.s.m. is required. This will depend on the type of filter used.

The type of digital filter discussed in section 3.1.2 will be used. The number of coefficients used (order) will affect the filter's frequency response, which in turn will affect the amount of noise passed on to the second modulator. K is chosen to avoid overload of the second encoder.

A calculation is now performed to find the power of the noise signal applied to the second d.d.s.m. after the error signal has been filtered by different order filters (H(z)).

The input signal applied to the digital filter, which is the output of the first d.d.s.m., has been shown to contain two components; the sampled input signal (X(z)) and the sampled quantization noise component

(Q(z)). As these are both random signals the only method of differentiating between them is by considering their power spectra. It is possible to calculate the shape of the power spectrum of the noise produced by a d.d.s.m. Consider the z-domain representation of a d.d.s.m. as shown in Figure 3.4, it follows that:-

$$Y(z) = \frac{(X(z) - Y(z) \cdot z^{-1})}{(1-z^{-1})} + Q(z) \qquad 3.14$$

re-arranging to obtain Y(z), X(z) separately we obtain:-

$$Y(z) = X(z) + (1 - z^{-1}) \cdot Q(z) \qquad 3.15$$

This shows that the flat noise spectrum produced by the quantizer (Q) has become modified by the term $(1-z^{-1})$, which has the frequency response of;-

$$2 \left| \text{Sin}(\pi fT) \right| \qquad 3.16$$

Thus the power spectrum of the noise produced by the d.d.s.m. ($N_m(f)$) will have the form:-

$$N_m(f) = C_o \text{Sin}^2 (\pi fT) \qquad 3.17$$

The total noise power (V^2) will appear in the band 0 - $f_{m/2}$, so the constant C_o can be found using:-

$$\int_0^{f_{m/2}} C_o \text{Sin}^2(\pi fT)\, df = V^2 \qquad 3.18$$

from which we obtain:-

$$C_o = \frac{4E^2}{f_m} \qquad 3.19$$

Substituting this result into equation 3.17 we obtain:-

$$N_m(f) = \frac{4E^2}{f_m} \text{Sin}^2(\pi fT) \qquad 3.20$$

If we define the digital filters power transfer function, normalised to have unity gain at zero frequency as $P_Q(f)$, then the power spectrum (N(f)) out of the digital filter before subsampling is:-

$$N(f) = N_m(f) \cdot P_Q(f) \qquad 3.21$$

When N(f) is subsampled to a rate f_s, determined by the frequency response of the filter, and because the filter is not ideal the remaining noise in the band $f_s - f_m/2$ will be aliased into the band $0-f_s/2$ and added to the existing noise present in the message band. The total in-band noise N_s is then given by:-

$$N_s = \int_0^{f_{m/2}} N(f)\, df \qquad 3.22$$

Using this equation it is possible to obtain the resulting total in band noise power from using a particular digital filter.

The normalised power transfer function for a filter with a uniformly weighted set of coefficients is:-

$$P(f) = \frac{\mathrm{Sin}^2(m\pi fT)}{(m\pi fT)^2} \qquad 3.23$$

when a triangular set of coefficients are used we obtain:-

$$P(f) = \frac{\mathrm{Sin}^4(m\pi fT)}{(m\pi fT)^4} \qquad 3.24$$

substituting these expressions into equations 3.21 and 3.22 we obtain an expression for the total noise presented to the second d.d.s.m.:-

$$N_s = \frac{4E^2}{fm} \int_0^{f_{m/2}} \frac{\mathrm{Sin}^2(\pi fT) \cdot \mathrm{Sin}^2(m\pi fT)\, df}{(m\pi fT)^2} \qquad 3.25$$

when a uniformly weighted filter is used, a similar expression is obtained

as for the triangular weighted filter. In practice it is necessary to evaluate equation 3.25 numerically, where it is approximated by:-

$$\frac{N_s}{V^2} = \frac{8N}{m^2\pi^2} \sum_{n=0}^{n=N} \sin^2\left(\frac{\pi n}{2N}\right) \cdot \sin^2\left(\frac{\pi n M}{2N}\right) \cdot \frac{1}{n^2} \qquad 3.26$$

Evaluating the summation enables a comparison of the amount of noise power removed by the filter. The amount of the total noise power (V^2) which appears in the message band (N_s), can be expressed as a ratio and termed "interpolation advantage". The results of evaluating equation 3.26 for two types of filters at three different cut-off frequencies (determined by their order) are tabulated below.

	Interpolation Advantage		Cut off Frequency
Order of Filter (m)	Uniform Coeff. filter	Triangular Coeff. filter	First zero as a function of f_m
64	-33.23 dB	-42.22 dB	$f_m/_{64}$
128	-39.26 dB	-51.23 dB	$f_m/_{128}$
256	-45.28 dB	-60.25 dB	$f_m/_{256}$

Most of the aliased noise comes from the low frequency end of the modulators noise spectrum. This is shown in Figure 3.5, the power spectrum at the filter's output prior to sub-sampling.

The gain of d.d.s.m. 1 is set such that it can accept peak input signals without overloading. If both modulators are assumed identical then the ratio between their relative gains (K) is given by:-

$$K = \frac{\hat{s}}{\hat{e}} \qquad 3.27$$

$\hat{s}$ = peak input signal to d.d.s.m. 1

$\hat{e}$ = peak noise input to

The output of d,d,s,m, 1 consists of the approximation voltages used within the modulator which are ±V. So the total signal and noise power must be V^2. If the signal power is P_s then the total noise power is:-

$$E^2 = V^2 - P_s \qquad 3.28$$

If the input signal is assumed sinusoidal then its power will be $V^2/2$. Thus the noise power will also be $V^2/2$. Using the results of the numerical analysis to calculate Q, (the interpolation advantage), the R.M.S. noise voltage produced by d.s.m. 1 after filtering by the digital filter (H(z)) is given by:-

$$V_N = \sqrt{Q \frac{V}{2}} \qquad 3.29$$

V_N = R.M.S. Noise Voltage

Q = Constant determined numerically

However, d.d.s.m. 2 must be able to encode the peak of their error signal, and this can only be found if the crest factor for the noise is known. To continue this analysis, and to find an approximate value of K to allow a practical system to be built, a value for the crest factor must be assumed. A value for K could then be determined from equations 3.27 and 3.29.

$$K = \frac{V}{CN \sqrt{\frac{Q.V^2}{2}}}$$

CN = Crest factor of the noise

$$K = \frac{\sqrt{2}}{CN \cdot \sqrt{Q}} \qquad 3.30$$

If the noise is assumed Gaussian, then a crest factor of 3 can be assumed with a very low probability of higher noise signals occurring. This approximation allows a quantitative assessment of the system's performance to be made. Then theoretical estimates of the values of K possible using the different filters considered can be made by using equation 3.30. It is then possible to calculate the resulting decreases in noise using equation

3,13. These results are shown in the table below:-

	Theoretical value of K		Improvement in noise level	
Value of M	Uniform filter	Triangular filter	Uniform filter	Triangular filter
64	20,9	57.9	26.4 dB	35.2 dB
128	42.9	169	32.6 dB	44.5 dB
256	84,8	476	38.5 dB	53.5 dB

Since the proposed system is digital, multiplication and division by any quantity not in the form of equation 3.31 below:-

$$K' = 2^n \qquad n = \text{integer} \qquad 3.31$$

would require a dedicated multiplier. This can be avoided by making K equal to the nearest integer that will satisfy equation 3,31. Then scaling by K'can be accomplished by shifting the bit field of the output of the digital filter before applying it to the input of the second modulator.

3.2.3 Practical Limits on the Filters Frequency Response

So far the analysis has concentrated on the noise performance of the system. It is important to consider the frequency response of the six different filters and their effect on the systems performance.

The frequency response of the filters depends on the length of their weighting functions and is described by the following equations:-

$$H(f) = \frac{\text{Sin}(m\pi fT)}{(m\pi fT)} \quad \text{- for uniformly weighted coefficients} \qquad 3,32$$

$$H(f) = \frac{\text{Sin}^2(m\pi fT)}{(m\pi fT)^2} \quad \text{- for triangularly weighted coefficients} \qquad 3,33$$

Using these equations it is possible to calculate the frequency at which the first transmission zero occurs and the amount of attenuation introduced at the signal band edge. Assuming a sample rate of 4096 kHz and a message band up to 15 kHz the following results were obtained:-

		Attentuation at band edge	
Value of M	Frequency of the first zero	Uniform weighting coefficients	Triangular weighting coefficients
64	64 kHz	0.8 dB	1.6 dB
128	32 kHz	3.4 dB	6.8 dB
256	16 kHz	23.6 dB	47.2 dB

These results show that certain filters produce a significant in-band droop. This means that when a high frequency signal is applied to the system it will appear at the output of d.d.s.m.1 but not at the output of the digital filter, so when the filtered output is compared with the original input, this missing high frequency information will be reproduced in the error signal applied to the second modulator. At high signal levels this will cause overload. However, even small signal levels will produce an incorrect error signal which will be passed through the second modulator to the systems output where it will appear as additional noise, so it is necessary to restrict the order of filter used to values of m = 128 or less.

3.2.4 Calculating the Improvements in S/N

The overall improvement in the signal to noise obtained by using the error feed-forward technique is given by expression 3.4. If we assume the magnitude of the noise produced by each d.d.s.m. is identical, then the

theoretical improvement in the signal to noise can be calculated. These results are summarised for the four filters which produce negligible in-band attenuation in the table below:-

M	K	K'	Gain in S/N	Basic PSM S/N	Overall S/N
64	17.1	16	24 dB	63 dB	87 dB
128	34.5	32	30 dB	63 dB	96 dB
64	85.0	128	42 dB	63 dB	105 dB
128	24.1	256	48 dB	63 dB	111 dB

In this table K' represents the nearest integer which is a multiple of two approximately equal to K.

A value of K can be obtained assuming the digital filter is ideal. This analysis is carried out for the two values of M used and shown below for comparison.

Value of M	Interpolation Advan.	K	K'	Gain	Overall S/N
64	44.2 dB	76.8	64	36 dB	99 dB
128	53.3 dB	216.6	256	48.2	111

These figures show that although an ideal filter reduces the level of noise applied to d.s.m. the need to quantise K results in little overall improvement.

3.3.1 Construction of an Error Feed-Forward System

In the previous section all the viable filters were considered and a short list of practical combinations drawn up. To maintain maximum flexibility, the practical circuit uses a triangular filter which can be set at either M=64 or M=128. In the remaining design procedure values of

M=64, K=64 will be assumed. The simplified diagramatic representation of the error feed-forward system shown in Figure 3.3 cannot be implemented directly since no attempt has been made to compensate for circuit delays.

3.3.2 Compensating for the Circuit Delay

To ensure that the signals representing the main output and the error signal are always added in the correct phase two additional delay stages are required. These are incorporated in the diagram shown in Figure 3.6. When the input signal is subtracted from the filtered d.s.m. output it is necessary to delay the input signal by an amount equal to the delay introduced by the d.d.s.m. and filter circuits. A similar delay is necessary in the output of d.d.s.m.1 to ensure its output is in phase with the output of d.s.m. 2.

If we first consider the delay introduced by a d.d.s.m., which can be obtained from the transfer function given in equation 3.15, this shows that the d.d.s.m. introduces a delay of one clock cycle between the input and output signals.

A similar technique shows the delay introduced by the filter is:-

$$\text{Filter delay} = mT \qquad 3.34$$

This means that the delay required in each delay stage (D1, D2) to cancel that introduced by d.d.s.m. 1 and the filter is (m+1)T.

3.3.3 Equalising the System's D.C. Gain

Throughout the theoretical analysis all the constituent components were normalised to give a unity gain at D.C. To ensure that this is correct in the practical system the gain of each component requires compensation.

Setting z=1 in equation 3.15 shows the D.C. gain of a d.d.s.m. is unity, thus no compensation is required at this point.

The transfer function of the digital filter is given by:-

$$H(z) = \frac{(1 - z^{-m})^2}{(1 - z^{-1})^2} = \left| \frac{m\, z^{m=1}}{mz^{m+1} - m+1\, z^{m+2}} \right|^2 \qquad 3.35$$

Setting z=1 yields the D.C. gain as:-

$$\text{D.C. Gain} = \left(\frac{m}{m-m+1}\right)^2 = m^2 \qquad 3.36$$

Since this D.C. gain is completely predictable its effect can be compensated by shifting the bit field of the filter's output.

A complete schematic diagram of the overall feed-forward system is given in Appendix 3.

3.3.4 The Analogue Circuitry

The error feed-forward system's digital section produces two one-bit D.S.M. outputs. To complete the feed-forward loop these data streams need to be summed and the lower d.s.m. 2 output weighted by $^1/_K$.

The output of each digital d.s.m. is applied to a pre-filtering stage, as outlined in Section 2.2.5. The use of their circuit is two-fold:

(a) Provide sufficient filtering to allow conventional op-amps to carry out additional processing.

(b) The circuit is independent of unequal rise and fall times in the output of the d.s.m. modulation.

Once the data is pre-filtered the signals are applied to the summer stage. The summer circuit is shown in Figure 3.7. The output of the adder is arranged to be the weighted sum of the two data streams. Weighting and summation is spread over two stages to permit the slew-rate and input specification of the operational amplifier to be relaxed. It is necessary to ensure the group delay of each path is identical before summation takes

place, so that the two error signals contained in each data stream cancel. The analysis contained in Appendix 3 shows that component tolerances of 5% give an acceptable additional noise level of -94 dB due to imbalance in the group delay of the two paths.

The weighting by K of the two data signals is determined by the feedback network in the operational amplifiers, any error in the relative value of K will increase the noise level introduced at the coders output. To ensure this does not occur K must be maintained to within 1% of the theoretical value.

3.4.1 Performance of the Practical System

When a practical system was constructed, it proved impossible to obtain stable operation over the required range of input signals. This incorrect operation resulted from the inability to choose a value of K which allowed the second d.d.s.m. to encode the range of noise signals applied to it. The second encoder was either overloaded or unable to encode the level of noise presented to it from the digital filter. As these two effects occurred at different input signal levels, they are best explained by considering the operation of the system at these different levels.

3.4.2 Performance at High Signal Levels

When high signal levels are encoded by the feed-forwardsystem most of the signals energy passes through the top encoder, any error the top encoder makes in encoding is detected and presented to the second encoder for subsequent removal at the system's output. The error signal when an input signal of -6 dB is applied to the system is shown in Figure 3.8. The crest factor of this signal can be estimated as 2.96 indicating that the original approximations made in section 3.2 were correct. Operation of the circuit with input signals greater than -40 dB below peak closely follows the theoretical predictions.

3.4.3 Performance at Low Signal Levels

When low level signals (more than 40 dB below peak) are encoded by the system the previous situation no longer applies. Since the top d.d.s.m. has an encoding threshold of approximately -50 dB below peak, (obtained from the results in Chapter 2), most of the signal's energy should be encoded by lower d.d.s.m. This is consistent with the value of K selected at -36 dB below peak signal. Clearly the system should be able to function without the top encoder and give results 36 dB better than a single d.d.s.m.

Unfortunately the top encoder attempts to encode these low-level signals, and in the process produces a very poor signal to noise at its output. The error signal produced under these circumstances attempts to correct for this additional noise so instead of encoding the required input signal, the second encoder has to correct for the error introduced by the top encoder. The feed-forward system would still function correctly under the above situation provided the resulting error signal stayed within the encoding range of the second d.d.s.m., however, this is not the case. The noise spectrum produced by a d.d.s.m. when its input signal is below the theoretical encoding threshold contains a large amount of low frequency energy. This is illustrated in Figure 3.9 which shows the error produced for an input signal -60 dB below peak. The theoretical model used to predict the performance of a feed-forward system assumed the quantization noise spectrum increased in amplitude with increasing frequency, as described by equation 3.19. If most of the quantization noise produced by the top encoder occurs at low frequencies it will not be removed by the digital filter, so will pass un-attenuated into the second d.d.s.m. As the output of the filter is scaled by K, low frequency quantization noise can easily overload the second encoder. If this occurs then the noise produced by the top encoder cannot be cancelled by the lower encoder so it will appear at the system's output.

3.4.4 The Production of Low Frequency Q.N.

The production of this low-frequency noise by the top d.d.s.m. can

be explained by considering the operation of the d.d.s.m. The maximum voltage that can be encoded by the d.d.s.m. is V, which is also equal to the approximation signal. A change in the output of the d.d.s.m. is caused when the accumulator value equals the approximation voltage. The input signal is held constant for m d.d.s.m. clock periods during which it is repeatedly added into the accumulator. There will be a minimum input signal value which when accumulated over the m d.d.s.m. clock periods will not equal the approximation signal. If this occurs, then the output of the d.d.s.m. will be un-perturbed by that input sample. This is known as the low-level encoding threshold (X_{min}) which can be quantized as:-

$$X_{min} = \frac{V}{m} \qquad 3.37$$

The accumulator is not re-set at the end of each input sample, so the accumulated sum from the previous input sample is still present when the new input sample value is applied. Eventually the accumulated sum will equal the approximation signal and a change in output of the modulator will occur. The frequency at which this occurs was calculated in Chapter 2 (equation 2.27) for D.C. input signals. When low frequency input signals are applied consecutive input samples of similar magnitude can be assumed to be equivalent to D.C. over a few input samples. Then equation 2.27 can therefore be used to predict the level at which an input signal will cause a single change in output at a frequency inside the passband of the digital filter. This will occur for signal levels around -50 dB below peak. Thus any input signal with a high probability of signal levels around -50 dB will cause significant low-frequency quantization noise to be generated. These in-band noise components contain considerable power, since they are caused by low frequency pulses with a magnitude of V. If we consider a perturbation of the idle pattern due to one additional "logic 1" occurring every 125 µs (caused by an input signal 54 dB below peak), The additional

pulse has a width of $\frac{1}{f_m}$ with a period of 125 μs and is shown in Figure 3.10a This produces the frequency spectrum shown in Figure 3.10b, the fundamental frequency of the pulse lies well inside the message band so will not be attenuated by the digital filter. The amplitude of this fundamental component is $^{2V}/_{128}$ and when this is scaled by K it produces an amplitude of 2V which will overload the second encoder. This simple numerical example serves to illustrate the mechanism by which low amplitude input signals cause the proposed feed-forward system to be overloaded. In practice more complex in-band noise components will be produced which result in a poor S/N performance at low input signal levels.

3.4.5 Conclusions on the Error Feed-Forward System

The system described so far in this section has little practical value since it performs no better than a single d.d.s.m. This is because the noise spectrum produced by the d.d.s.m. changes its form according to the level of input signal applied. To accommodate this shift in spectrum it is necessary to reduce the value of K used, but this limits the usefulness of the system. Since the error feed-forward system is complex no further investigations were carried out to find a value of K which would enable the system to perform satisfactorily.

3.5.1 A Modified Feed-Forward System

The high level of low-frequency quantization noise produced by the top d.d.s.m. in the error feed-forward system outlined in the previous section can be reduced by restricting the range of input signals applied to it. This can be achieved by disconnecting some of the lower bits of the input signal from the input to the top encoder. This arrangement is shown in Figure 3.12. This has the effect of allowing the top encoder to switch off whenever the input signal falls below its encoding threshold, leaving the bottom encoder free to encode the lower bits of the input signal. When this occurs the filtered output of the top encoder is zero, so the error

signal is identical to the lower bits of the input signal. Experiments showed that the best results are obtained by restricting the input to the top encoder to 7-bits. Under these conditions the digitally filtered output of the top encoder was always identical to the applied input signal. The next section shows that using this scheme it is possible to remove the digital filter altogether.

3.5.2 A Residual Error Encoder

The error feed-forward principle requires the detection of the error produced by the first modulator, its subsequent re-modulation and subtraction from the first modulators output. A considerable reduction in the system's complexity could be achieved if the error signal produced by the first modulator could be predicted in advance, removing the need for its detection.

It is possible to adjust the range of input signals applied to the top encoder such that it produces a unique output code for every possible input signal level. The results obtained for the d.d.s.m. used in Chapter 2 indicated they had good linearity for input signals over a reduced dynamic range. Using equation 2.12 it is possible to show that a unique output code can be produced by the modulator, provided the residual error at the end of M clock cycles (I(n)) is equal to the original residual (I(n-m)) at the beginning of the input sample period. Equation 2.12 then becomes:-

$$\sum_{i=n-m}^{i=n} X_i = \sum_{i=n-m}^{i=n} Y_i \qquad 3.39$$

Since Y_i is either 1 or 0 the summation of Y over M clock periods must be quantized in steps of 1 from a minimum of 0 to a maximum of M. So to satisfy equation 3.39 X_i must be similarly quantized. That is, the input signal must be quantized to B bits where:-

$$B = \log_2(M) \qquad 3.40$$

If these conditions are fulfilled and the initial residue (I(1)) is pre-set to zero, the output sequence generated for each input sample will be independent of all previous samples and unique to that particular input level.

Taking some practical values which will satisfy equation 3.39, a clock rate of 4096 kHz is required to encode 7-bit P.C.M. sampled at 32 kHz. It is now possible to predict the error signal since it would always be equal to the difference between the P.C.M. input sample and the signal applied to the top encoder. This difference is the residual between the true P.C.M. input signal applied to the system and that part of it applied to the top encoder.

3.5.3 A Practical Residual Error Encoder

Now the idea of a residual error signal has been developed, the residual error encoding concept can be outlined with reference to a 14-bit P.C.M. system. A diagram of this system is given in Figure 3.11.

A residual error signal is now derived, without the need for a digital filter, by comparing the pre- and post-quantized representation of the input signal (x(n)). The result (q(n)) is scaled by K and applied to a second digital d.s.m. As the digital input signal is already quantized both x(n) + q(n) and K.q(n) can satisfy equation 3.39. The overall output of the system will be:-

$$y(n) = (x(n) + q(n)) - {}^{1}/_{K}\ (K.q(n)) \qquad 3.41$$

output of d.d.s.m. 1 output of d.d.s.m. 2

which reduces to:-

$$y(n) = x(n) \qquad 3.42$$

A practical realization of Figure 3.11 is particularly simple since the quantization of the input signal to form the residual error signal can be

achieved by discarding the appropriate number of bits at the input to the first d.d.s.m. The discarded bits then form the residual error signal, which is applied to the input of the second d.d.s.m. The circuit then becomes that shown in Figure 3.12. The value of K is determined by the difference in the weighting between the signals applied to the top and bottom encoders. In the 14-bit system described $K = 2^7 = 128$.

3.5.4 The Performance of the Residual Error Encoder

The series of practical measurements carried out on the residual error encoder described in Figure 3.12 show that it performs better than any of the previous systems examined. Measurements of the signal to noise at different signal levels, are shown in Figure 3.13, indicate close agreement with the theoretical performance of 14-bit P.C.M. over most of the required dynamic range. Some additional noise is introduced at high signal levels, indicating some noise is introduced by the d.d.s.m. A further indication that some noise is introduced while the signal is encoded is shown in the level of harmonics produced by the input signal. These are tabulated in Table 3.1. Tests carried out using musical signals indicated the presence of considerable program modulated noise. This noise was found to be harmonically related to the input signal and more prominant at high signal levels.

3.5.5 The Spectrum of the D.S.M. Output

To understand the cause of the additional noise components, which result in the program modulated noise described in the previous section it is necessary to consider the output frequency spectrum produced by a d.d.s.m.

It has been shown that every input sample applied to a d.d.s.m. (provided it satisfies equation 3.39) produces an output sequence which comprises of a series of m pulses of amplitude V with a unique pattern. If for simplicity, we consider D.C. input signals the output pattern produced by the modulator will repeat at the input sampling frequency since this is

equal to m modulator clock periods. The spectrum produced is a series of lines whose amplitudes change according to the input signal level selected.

A good example of this spectrum is shown in Figure 3.14a where the input signal used caused the modulator to produce a single pulse over the period T. In this spectrum the resolution used does not permit the individual lines to be seen. A spectrum using an increased resolution over a reduced frequency range is shown in Figure 3.14b. These spectral components occur for a constant input signal only, and can be termed "main-lines". The lowest frequency main line will occur at $^1/_T$, which for the system described is 32 KHz, well outside the message band.

It is now convenient to extend this analysis to low frequency input signals. Consider an input signal with a period T_x, it will consist of a number of sample and hold input signals. Each of these levels will produce a sequence of m output pulses, termed a "block" of data. A periodic signal will be totally described by an integer number (P) of these blocks of data, where P can be evaluated from:-

$$P = \frac{T_x}{T} \qquad 3.42$$

These blocks of data are arranged serially, this concept is illustrated in Figure 3.15a. The spectrum produced by this set of blocks will also be a line spectrum whose lines are spaced at $^1/_{T_x}$. These lines are therefore present in the message band as noise.

Low frequency signals have long periods so the number of blocks of data describing them will be correspondingly large. The amplitude of these signals will be changing slowly so the pulse patterns contained in successive blocks will be similar. This results in a significant component of the sample frequency and its harmonics ($^1/_T$) being present in the spectrum of low frequency signals. The in-band lines which do occur, are at a low level. As an example, Figure 3.15b, shows the spectrum produced

by a 500 Hz input signal.

The period of a high frequency input signal will be short so the number of blocks of data describing this signal will be small. The pattern of pulses contained in these data blocks will be unrelated since the input samples they represent will differ greatly. As a result of this the lines spaced at the signal frequency will become dominant and the main lines become suppressed. This result is verified in the spectrum shown in Figure 3.15c, which is produced by an 8 KHz input signal. In summary the output spectrum of a d.d.s.m. when encoding periodic signals has been shown to consist of a line spectrum with in-band components. The magnitude of these in-band components depends on the amplitude and frequency of the input signal. As the period of the signal increases the separation of the individual lines reduces, so when a periodic signal is considered the period becomes very large so in the limit as $T_x \to \infty$ the line spectrum will become continuous.

3.5.6 Calculating the Magnitude of the In-band Harmonics

Having established that in-band frequency components can be generated by the d.d.s.m. it is necessary to calculate their amplitude to see how they limit the performance of the system. The practical results obtained in section 3.5.4 show that additional low frequency harmonics are produced at levels of -60 dB below peak input signal. Calculating the levels of the harmonics predicted in the previous section would confirm these practical results. To calculate the magnitude of each harmonic it is necessary to calculate the complete Fourier series of a periodic set of "blocks" of data. Taking, for example, a 500 Hz sinusoidal signal it would be necessary to calculate the fourier series of 64 blocks of 128 possible pulses. Evaluating this analytically is impractical, since no simple relationship exists between the input signal and the fourier series of the output pulses. Evaluating a high frequency input signal, which would generate fewer blocks of data, is less informative since few harmonics would fall inside the message band.

It is possible to evaluate the output spectrum numerically by simulating the operation of a d,d,s,m, on a computer and taking the fourier transform of the output sequence produced. Since the residual error encoder under review contains two d,d,s,m, the simulation was restricted to the top encoder only. Although the lower encoder will also produce in-band harmonics, their amplitude will be reduced by the scaling factor K to an insignificant amount.

The simulation program generated a 7-bit P,C,M, signal which was stored in an array. A Fourier transform of this input data was taken, and the level of each harmonic calculated. The harmonic distortion here is due only to the initial quantization. The input data was then applied to a simulated version of the d,d,s,m. A Fourier transform of the output sequence produced was taken and the level of each harmonic calculated again. The power contained in some input signal harmonics differed from the corresponding output signals harmonic power levels. This difference is attributed to the presence of an additional harmonic component generated by the encoding process. The series of harmonics contained in the output sequence can be considered as containing two separate components:-

1. The line spectrum representing the input signal,
2. The line spectrum produced by the encoder.

In the residual error encoder the harmonics contained in 1. will be reduced by the signal produced by the second encoder. The harmonics contained in 2. will not be reduced, and will appear at the output of the system.

The results of the simulation are summarised in the following table, (Table 3.2). A 500 Hz peak input signal was considered and the first 10 harmonics evaluated. The difference between each input and output harmonic was calculated and attributed to noise introduced by the coder. These results show that the magnitude of the harmonics introduced by the encoder occur at levels around -60 dB below peak signal. This indicates

that the encoder introduces additional harmonic distortion at approximately the same order of magnitude as that observed practically. Some differences are likely to occur because the samples used in each case are different. The simulation program does not take account of the finite rise and fall times in the output pulse pattern and this is likely to result in a slightly different Fourier series from the real system.

The results obtained from the residual error encoder have demonstrated its ability to improve the performance of a simple d.s.m. A fundamental limitation of d.s.m., the production of low-level harmonics within the message band, has been demonstrated and quantified. The performance of the system is insufficient for the conversion of 14-bit P.C.M. into an analogue signal, but the technique is suitable for D/A conversion of lower resolution signals.

	Signal Level			
Harmonic No.	0dB	-6 dB	-12 dB	-18 dB
1	0	0	0	0
2	-59 dB	-72 dB	-72 dB	-72 dB
3	-46 dB	-67 dB	-70 dB	-73 dB
4	-64 dB	-76 dB	-76 dB	-80 dB
5	-58 dB	-70 dB	-70 dB	-72 dB
6	-69 dB	-71 dB	-70 dB	-70 dB
7	-72 dB	-71 dB	-75 dB	-76 dB
8	-69 dB	-76 dB	-88 dB	-73 dB
9	-70 dB	-80 dB	-76 dB	-70 dB
10	-72 dB	-75 dB	-75 dB	-78 dB
Total Harmonic Distortion	0.01%	0.0022%	0.0019%	0.0019%

Table 3.1

Harmonic Number	Input Spectrum	Output Spectrum	Noise Spectrum
1	0 dB	0	-
2	-66 dB	-65 dB	-71.8 dB
3	-54 dB	-54 dB	-
4	-68 dB	-64 dB	-66.2 dB
5	-65 dB	-65 dB	-
6	-50 dB	-51 dB	-56.8 dB
7	-53 dB	-53 dB	-
8	-63 dB	-60 dB	-63.0
9	-57 dB	-57 dB	-
10	-64 dB	-61 dB	-64 dB

Table 3.2

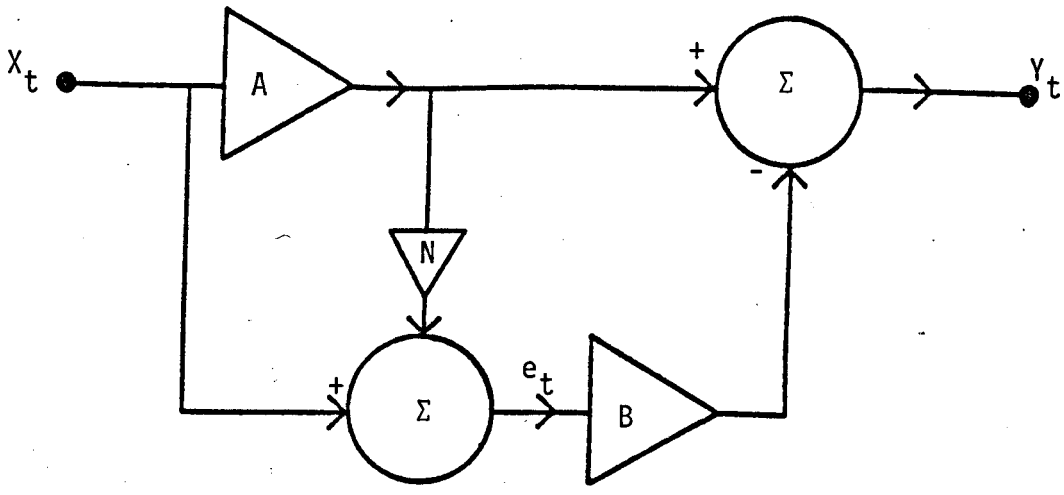


Figure 3.1 The error feed-forward system proposed by Black.

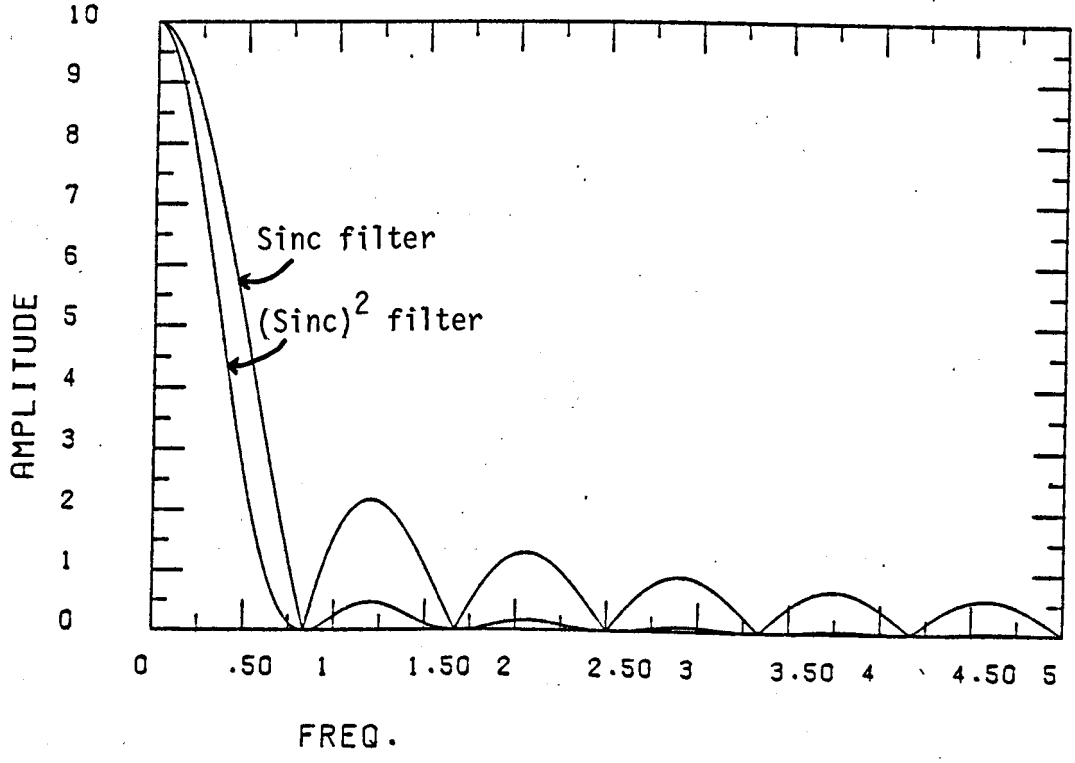


Figure 3.2 Frequency response of the filters.

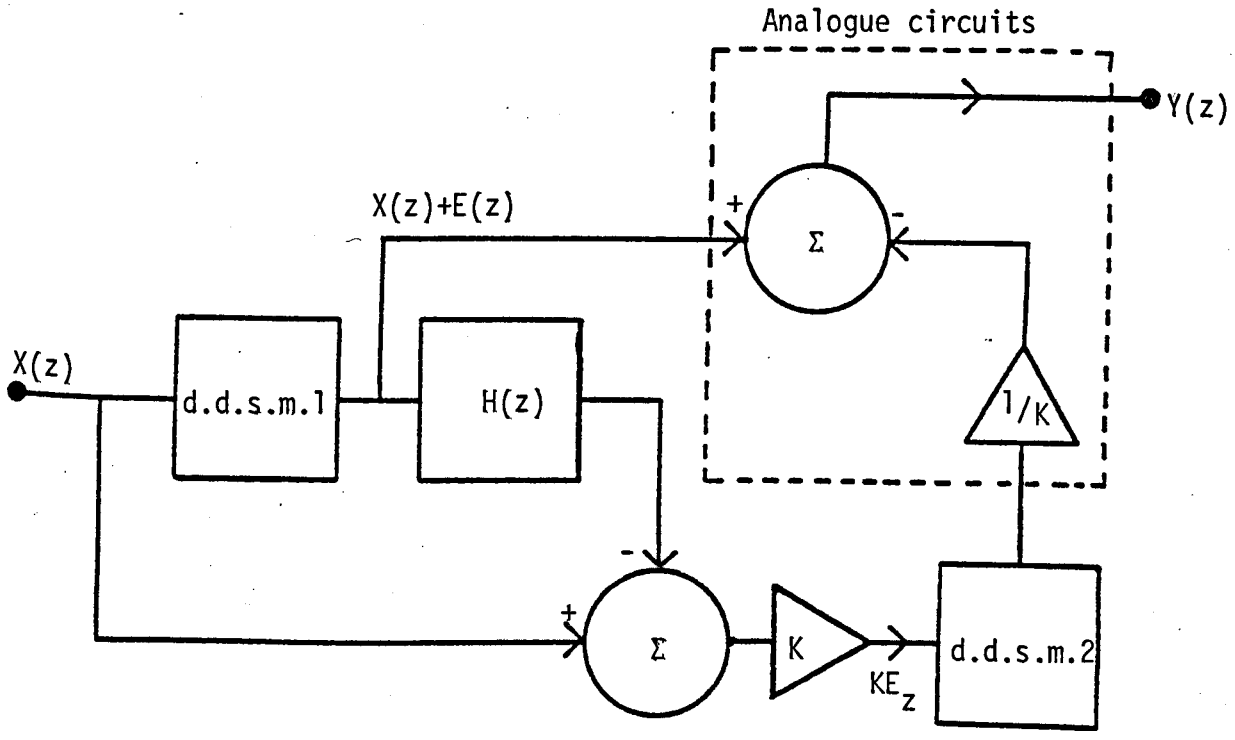


Figure 3.3 Proposed error feed-forward system.

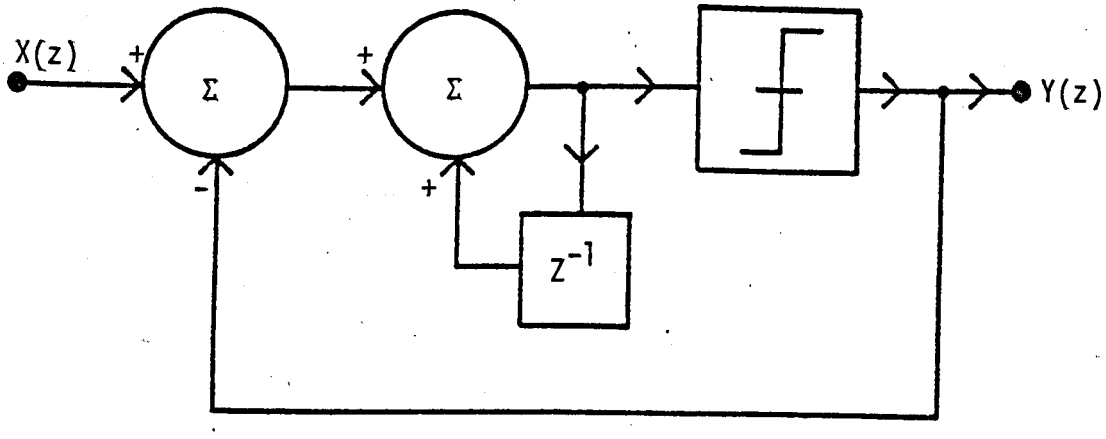


Figure 3.4 Z-domain representation of d.d.s.m.

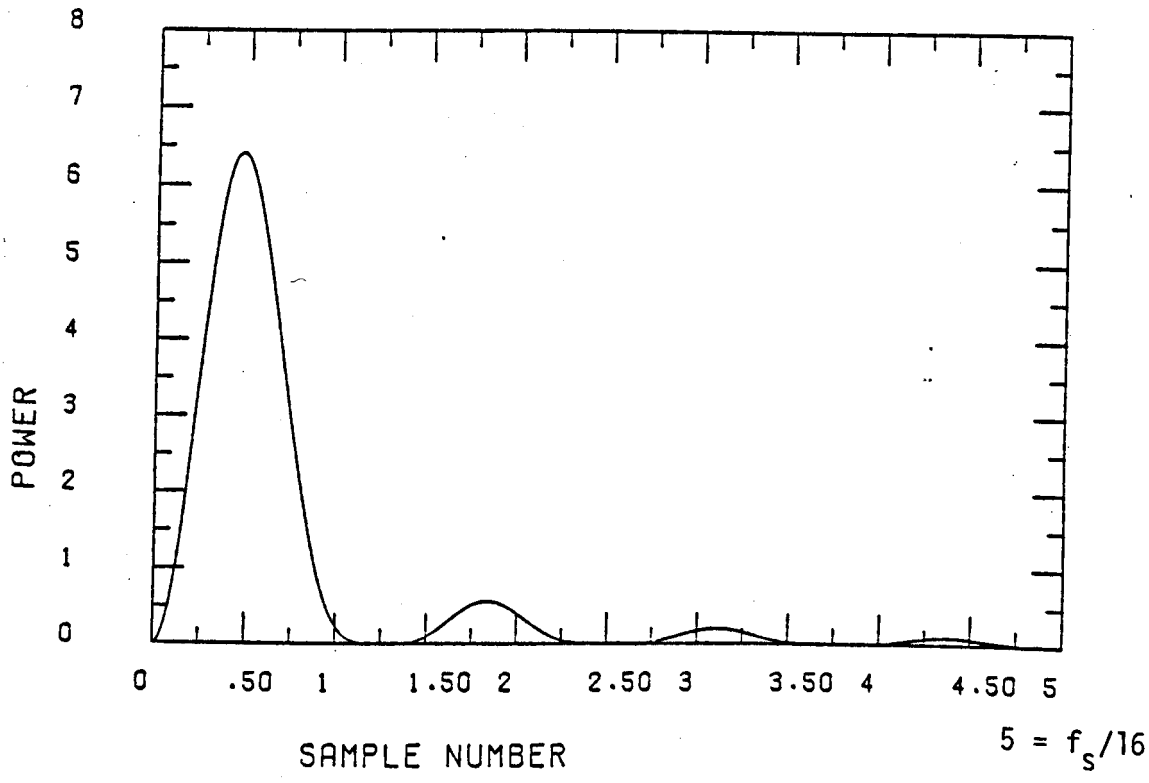


Figure 3.5 The power spectrum of the noise produced by the D.S.M. when filtered.

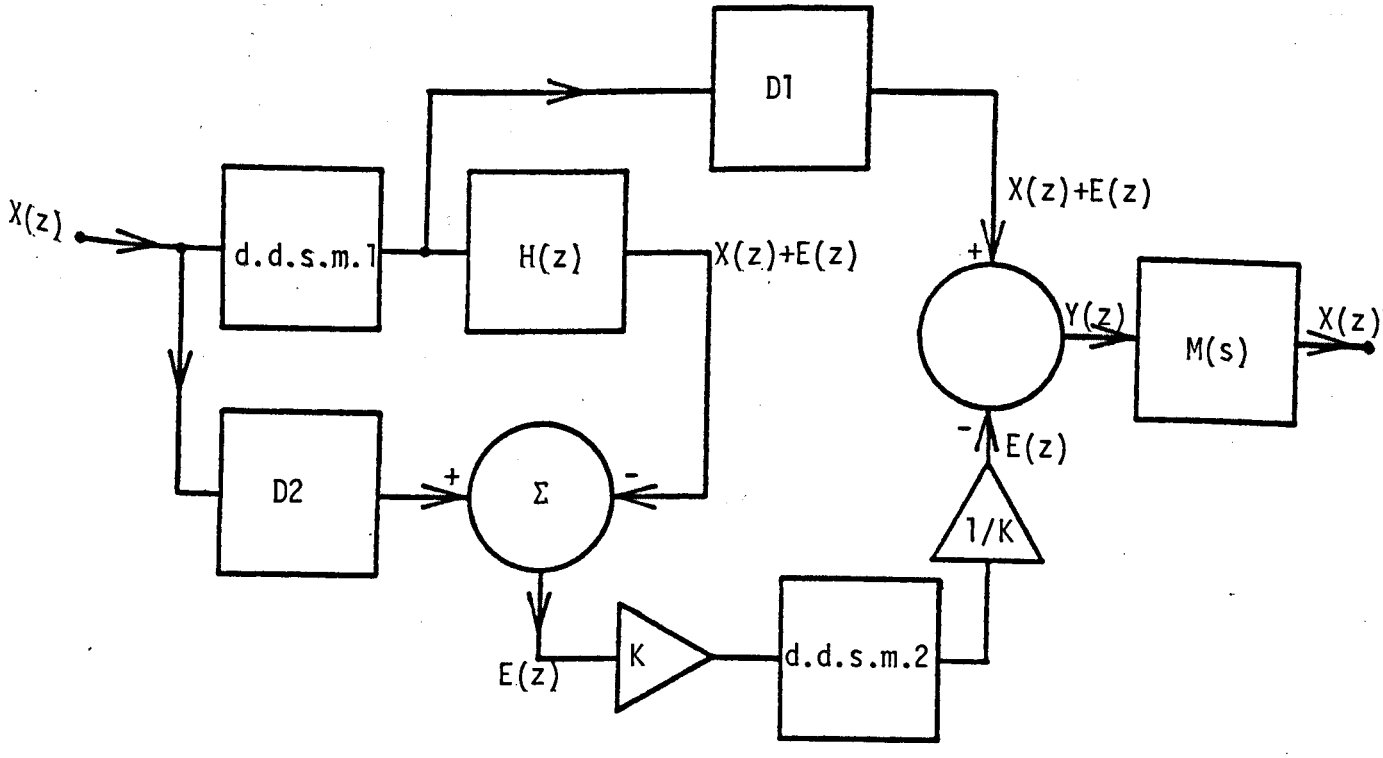


Figure 3.6 Practical error feed-forward system incorporating the circuit delays.

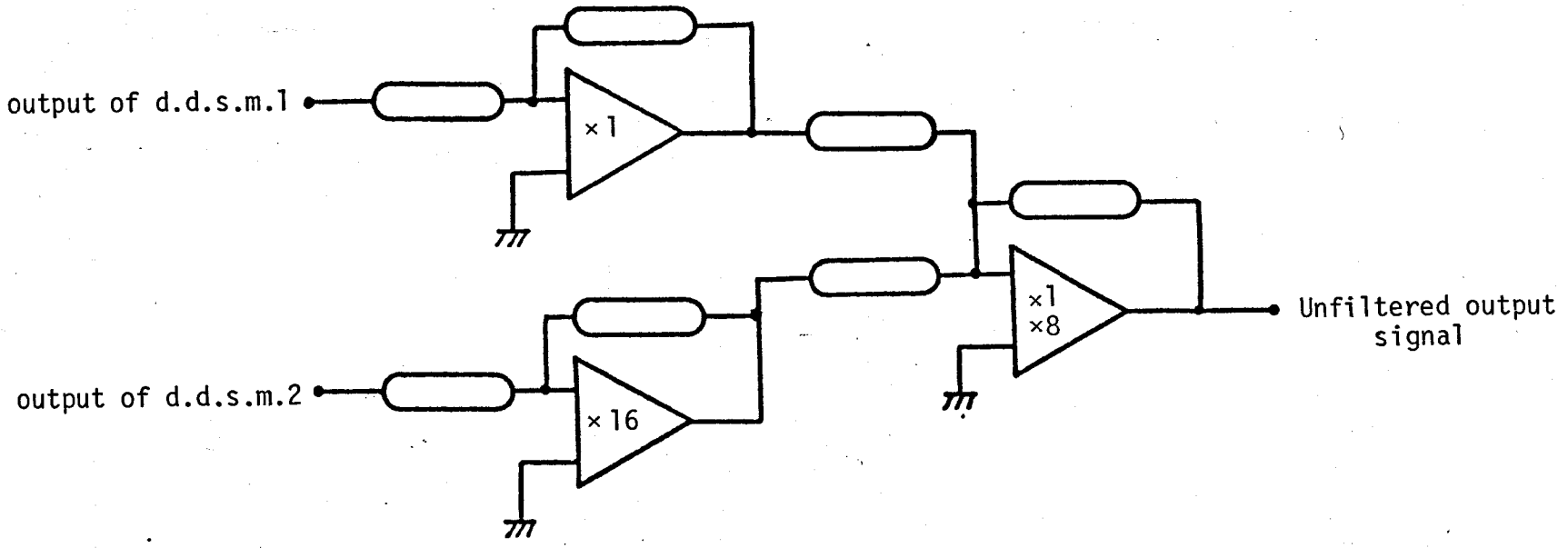


Figure 3.7 Analogue summer circuit, used to combine weighted D.S.M. outputs.

Figure 3.8 Error signal produced by the D.S.M. with an input signal of -6 dB.

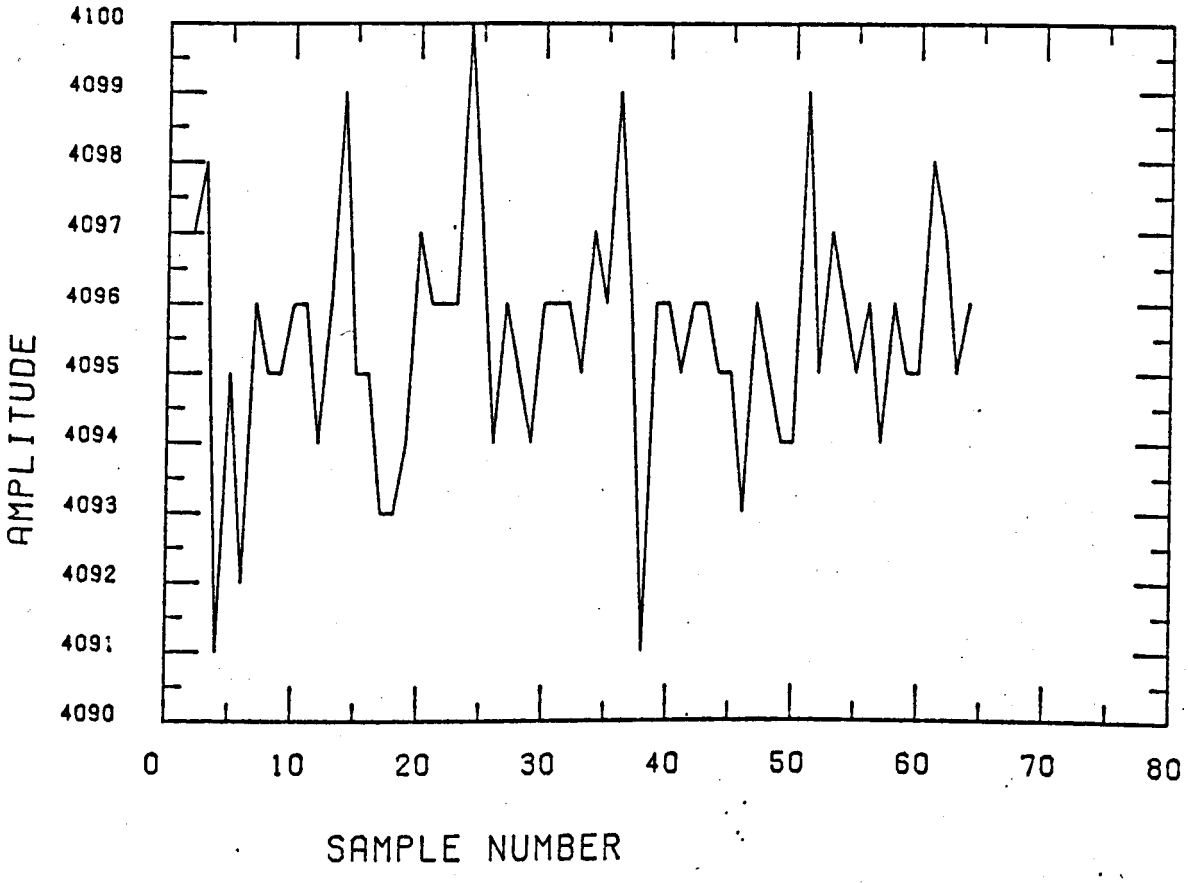
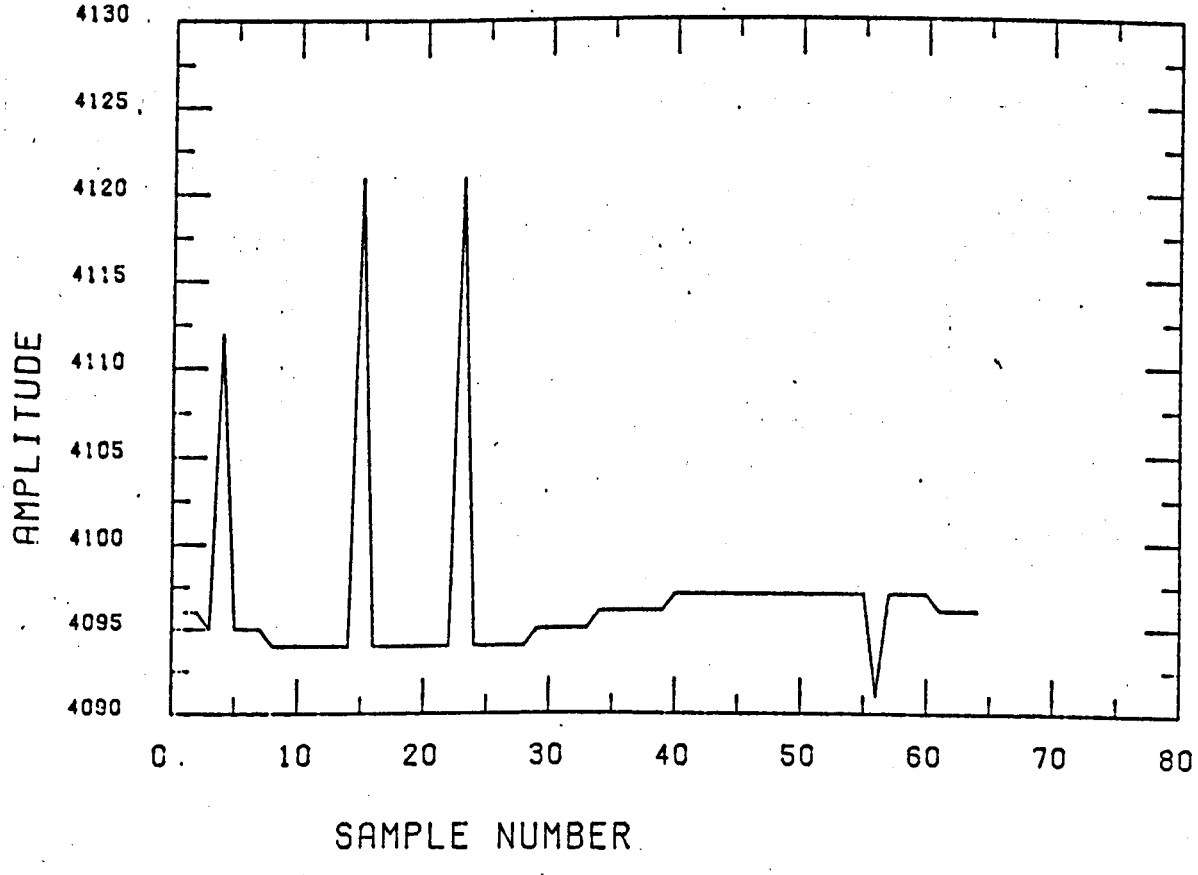


Figure 3.9 Error signal produced by the D.S.M. with an input signal of -60 dB.



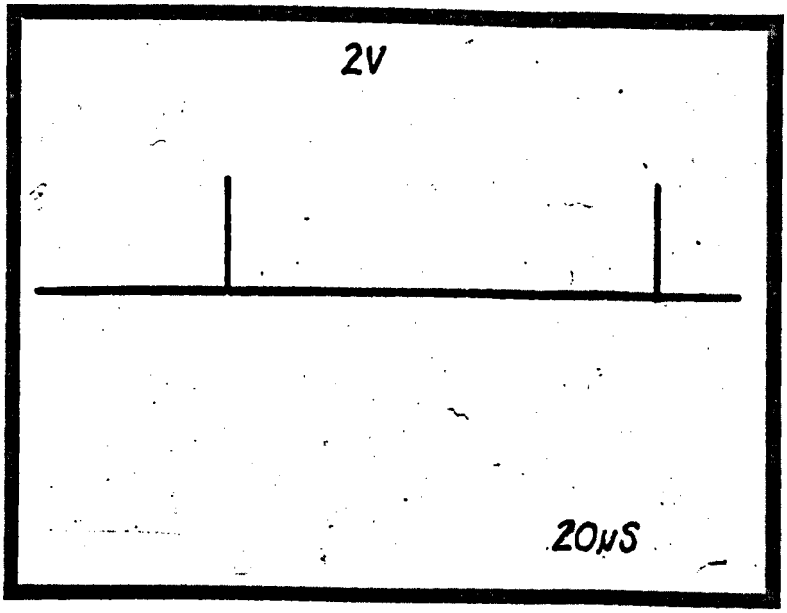
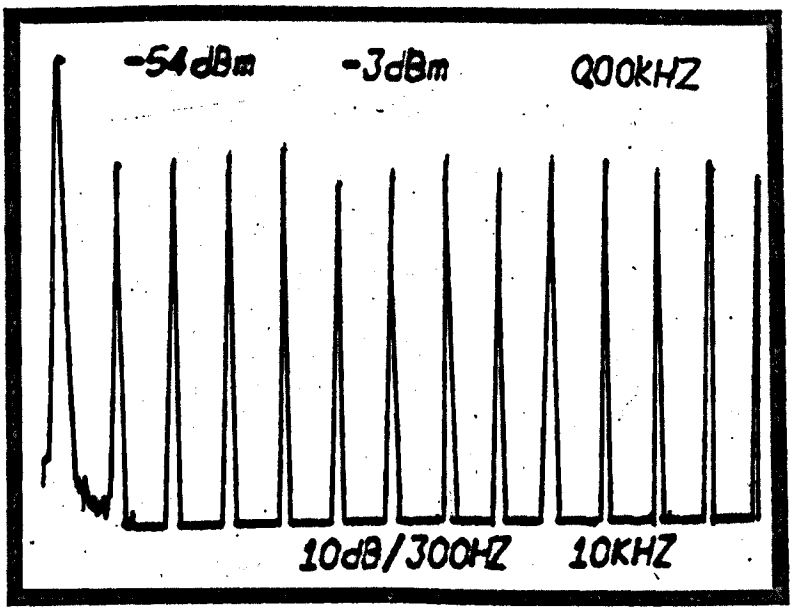


Figure 3.10a An example of a low frequency pulse produced by the d.s.m.



Vert. scale
10 dB/0.8 cm

Horiz. scale
10 kMz/0.8 cm

Figure 3.10b The resulting spectrum of Figure 3.10a.

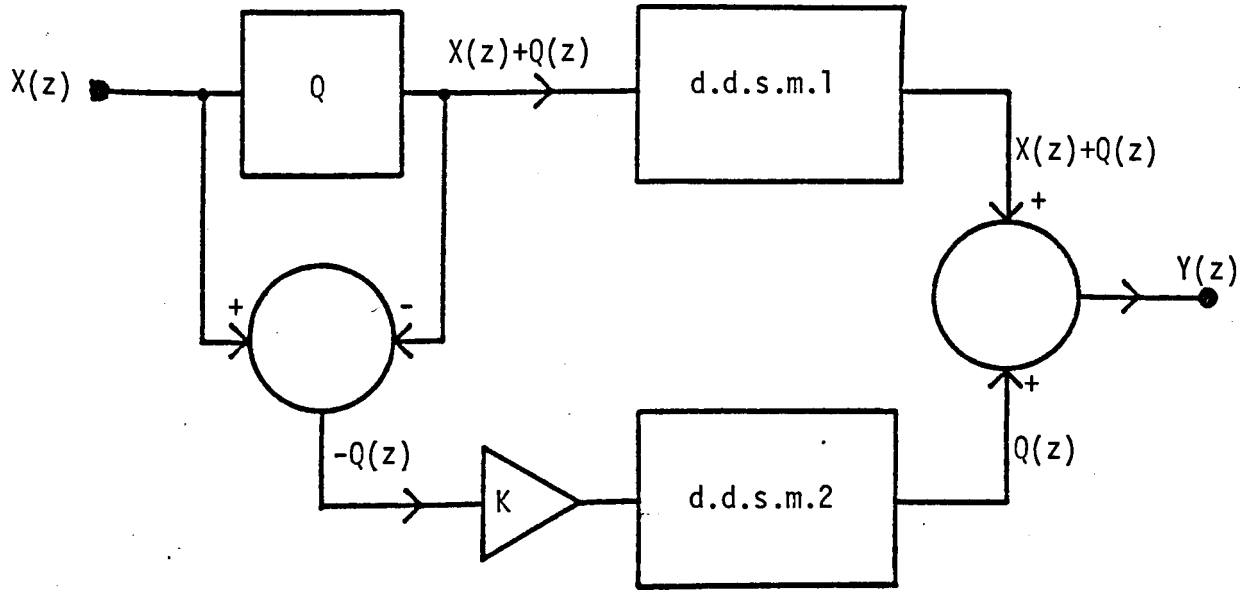


Figure 3.11 Block diagram of the proposed residual error encoder.

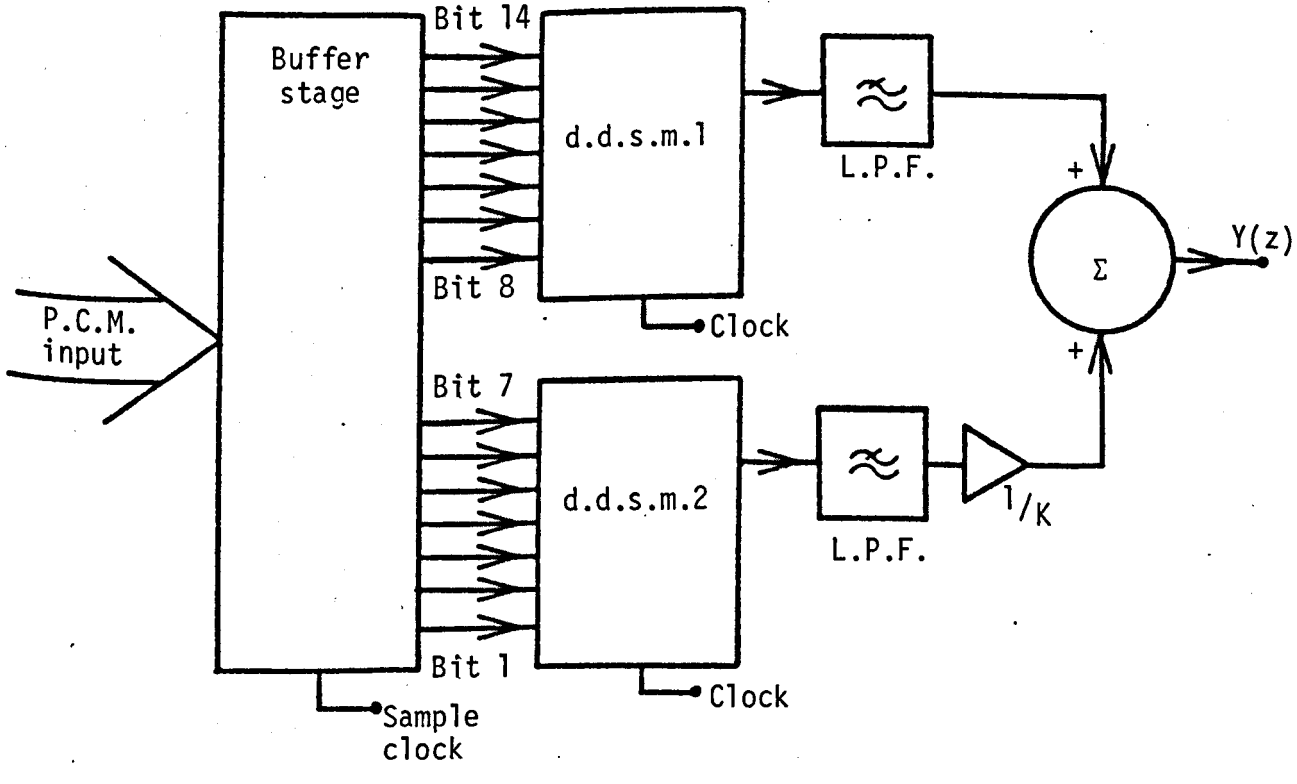


Figure 3.12 Simplified practical circuit of the residual error encoder.

SIGNAL TO NOISE PERFORMANCE

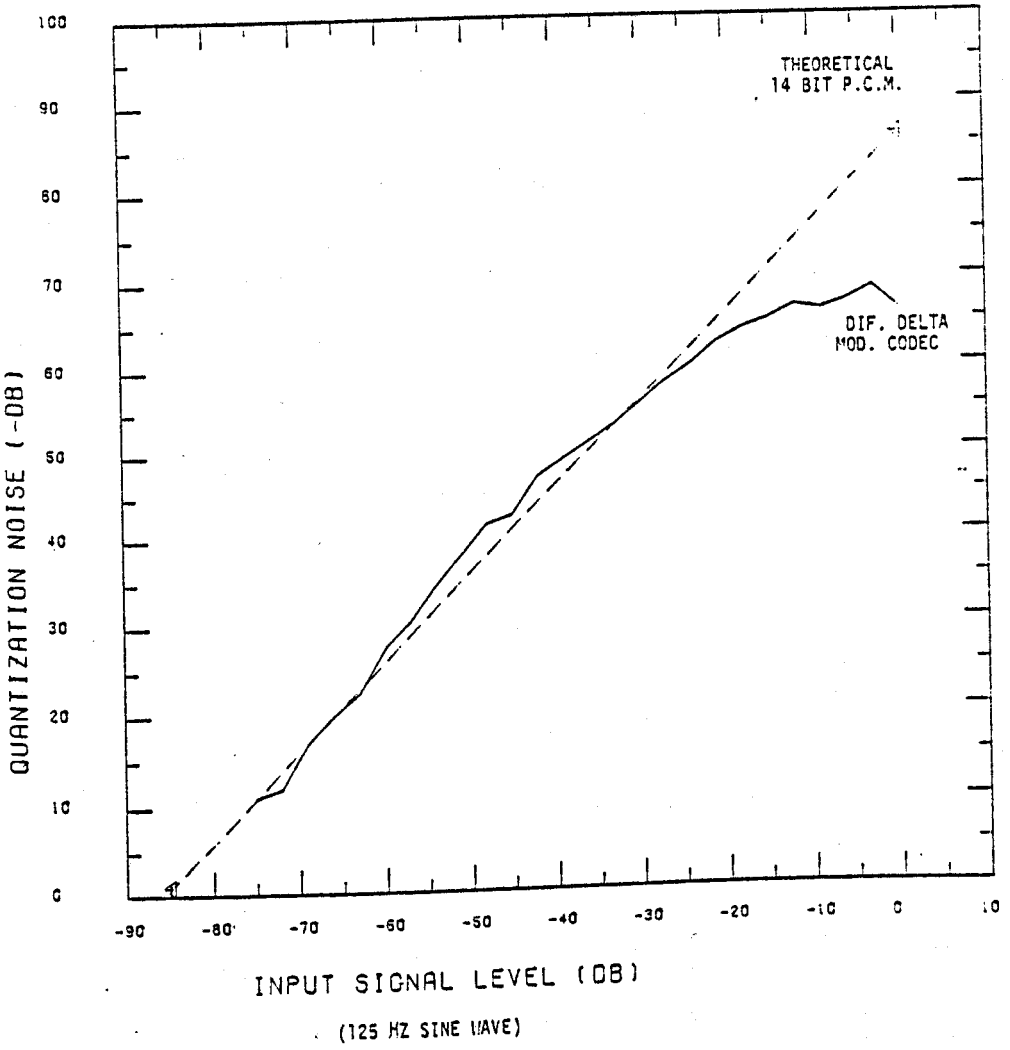
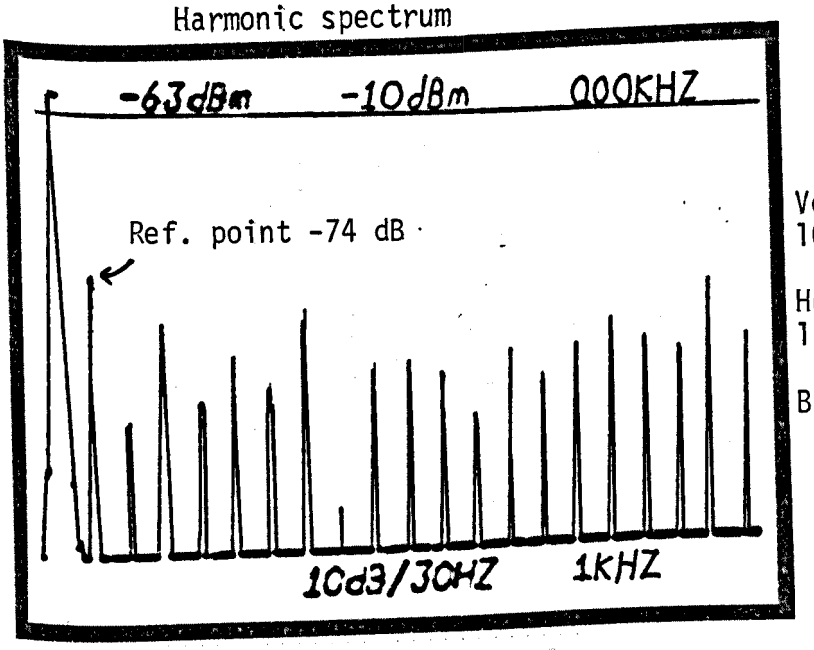


Figure 3.13 Noise performance of the residual error encoder.

Harmonic spectrum

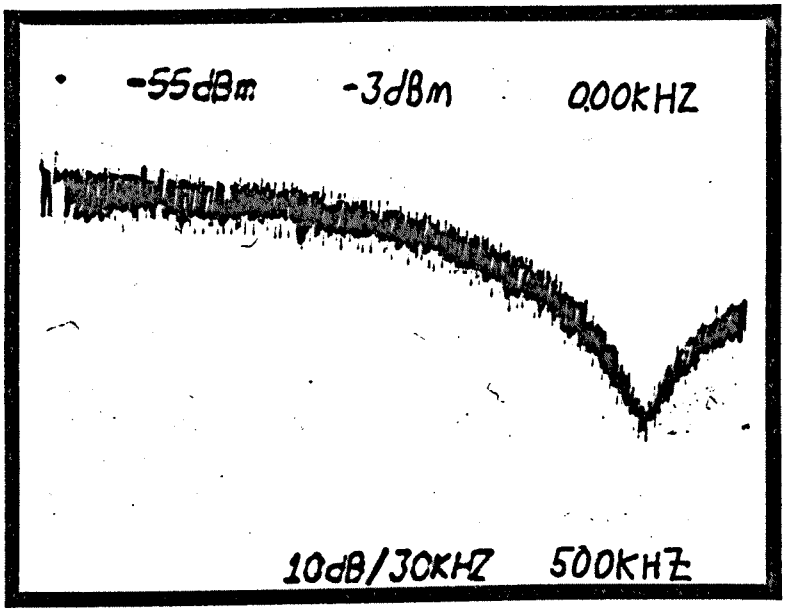


Vert. scale
10 dB/0.8 cm

Horiz. scale
1 kHz/0.8 cm

Bandwidth
30 Hz

Fundamental	=	- 6 dB
2nd harmonic	=	-94 dB
3rd harmonic	=	-80 dB
4th harmonic	=	-90 dB
Idle channel	=	-90 dB

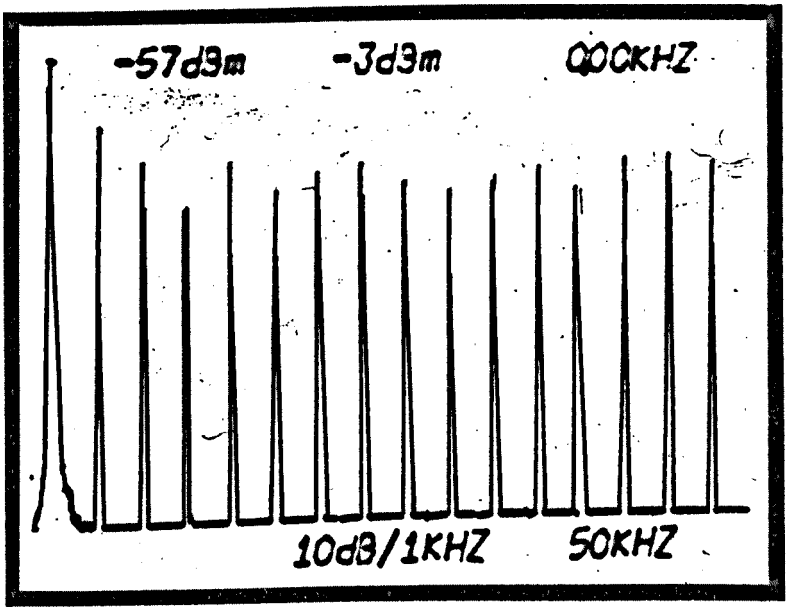


Vert. scale
10 dB/0.8 cm

Horiz. scale
500 kHz/0.8 cm

Bandwidth
30 kHz

Figure 3.14a Spectrum of the D.S.M. output when a small D.C. signal is applied.

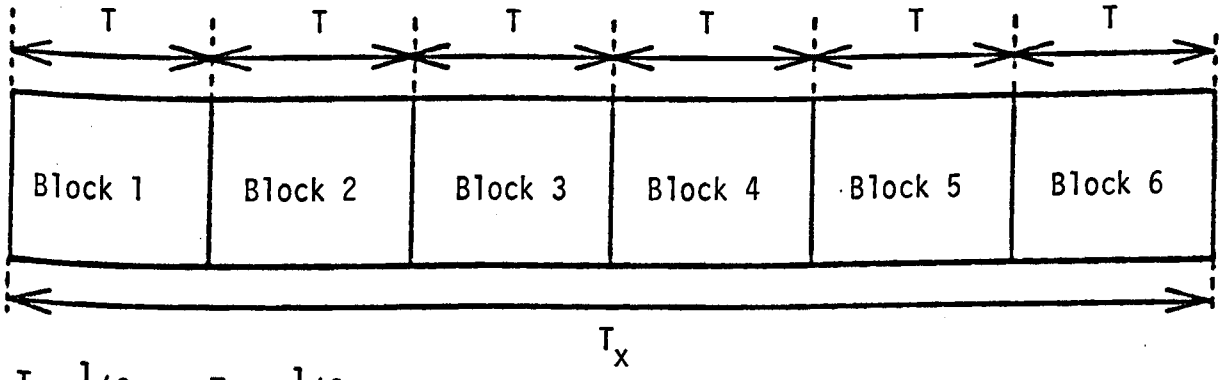


Vert. scale
10 dB/0.8 cm

Horiz. scale
50 kHz/0.8 cm

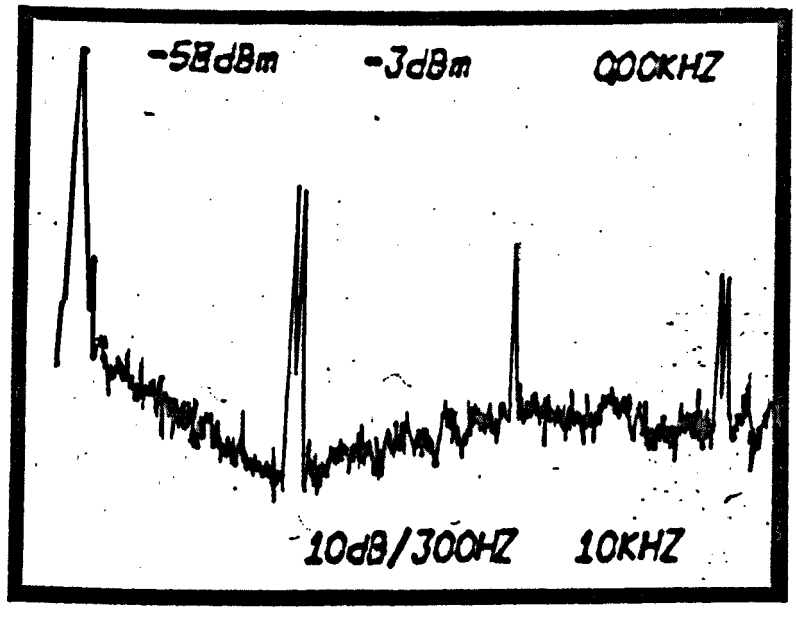
Bandwidth
1 kHz

Figure 3.14b The same spectrum with increased resolution.



$T = 1/f_s$; $T_x = 1/f_m$

Figure 3.15a Illustration showing the formation of a series of data blocks representing a periodic signal.

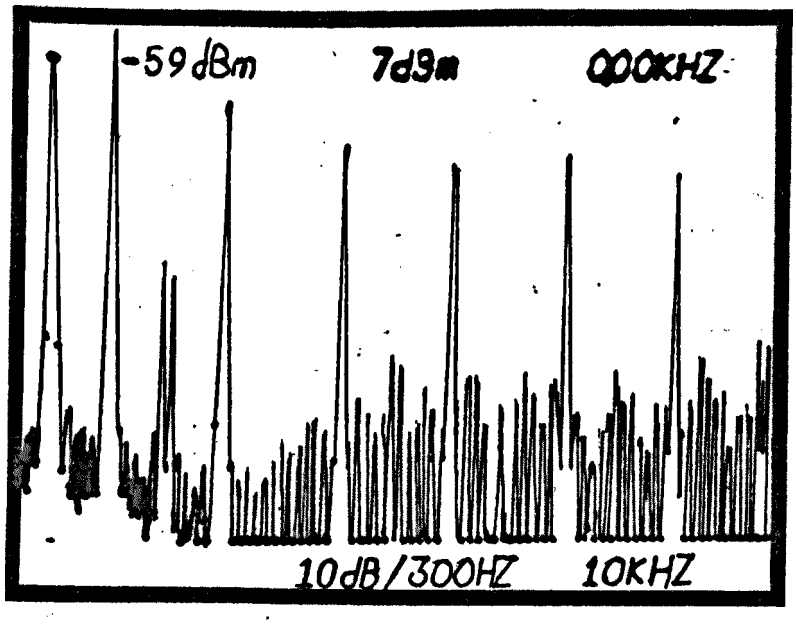


Vert. scale
10 dB/0.8 cm

Horiz. scale
10 kHz/0.8 cm

Bandwidth
300 Hz

Figure 3.15b Low frequency signal spectra



Vert. scale
10 dB/0.8 cm

Horiz. scale
10 kHz/0.8 cm

Bandwidth
300 Hz

Figure 3.15c High frequency signal spectra

CHAPTER 4

HIGHER ORDER DELTA MODULATORS

One method of improving the performance of d.d.s.m. is to increase the order of the filter contained in the feedback loop. The first part of this chapter reviews the work of Tewksbury and Hallock (Ref. 4.1) in developing oversampled high order predictive and noise shaping coders. Their results are then used to develop a second order noise shaping decoder suitable for digital audio applications.

4.1.1 Oversampled Linear Coders

The linear d.s.m. system previously described can be considered as the simplest of a general class of linear feedback oversampled encoders. A general linear feedback system is shown in Figure 4.1. In this system the input signal (S_n) is applied to a feedback loop containing a feed-forward filter (B(z)) and a feedback filter (C(z)). The z-transform of the input sequence is related to the output sequence by:-

$$Y(z) = \frac{B(z).S(z) + Q(z)}{1 + B(z)\,C(z)} \qquad 4.1$$

Q(z) = Transform of quantization error

S(z) = Transform of input signal

Y(z) = Transform of output signal

To decode the output from the encoder it must be passed through a decoding filter (D(z)) to produce S(z)*, i.e.

$$S(z)^* = Y(z) \,.\, D(z) \qquad 4.2$$

This ensures the correct frequency transfer characteristic between the input and output of the coder. Substituting for Y(z) from equation 4.1 in equation 4.2 the transform of D(z) is:-

$$D(z) = \frac{1 + B(z)\ C(z)}{B(z)} \qquad 4.3$$

The output of the coder-decoder pair is then given by:-

$$S(z)^* = S(z) + \frac{Q(z)}{B(z)} \qquad 4.4$$

It is convenient to define two different types of feedback systems, known as predictive coders and noise shaping coders. In a prediction system, B(z) and C(z) are chosen to allow the feedback loop to predict the level of input signals applied and therefore reduce the dynamic range of the coder contained within the feedback loop. In the noise shaping coder B(z) and C(z) are chosen to reduce the in-band coding noise power produced by the coder.

4.1.2 Predictive Coders

Predictive coders use a prediction filter (Hp*(z)) which affects both the input signal and the noise produced by the quantizer (Q(z)). A general predictive coder has the form:-

$$Y(z) = (S(z) + Q(z)) - Hp^*(z)\ (S(z) + Q(z)) \qquad 4.5$$

This has the more convenient form of:-

$$Y(z) = Hp(z)\ (S(z) + Q(z)) \qquad 4.5$$

since $Hp^*(z) = (1 - Hp(z))$

The coefficients of Hp(z) are chosen to reduce the error in predicting the input signal level. The constraints on B(z) and C(z) are necessary to ensure that equation 4.1 simplifies to the form of equation 4.6 which can be calculated as:-

$$B(z) = 1$$

$$C(z) = \frac{1 - Hp(z)}{Hp(z)} \qquad 4.7$$

Modulation methods such as D.M. and differential P.C.M. are forms of predictive encoding.

Substituting for B(z) and C(z) in equation 4.3 gives the required transfer function for D(z) in a predictive system.

$$D(z) = {}^{1}/_{Hp(z)} \qquad 4.8$$

So to decode the output of a predictive system a filter of similar complexity to the prediction filter is required. This limits the usefulness of predictive systems as an intermediate code in the construction of D/A converters. Since the added complexity of the decoder, which would need to be realised in analogue hardware increases the need for precision analogue components. The principle of using an intermediate code requires the removal of analogue circuitry at the expense of increased digital hardware.

4.1.3 Noise Shaping Coders

The principle concept in a noise shaping encoder is to choose the transfer functions of C(z) and B(z) so they remove the in-band quantization noise produced by the quantizer, without affecting the input signal. Therefore noise shaping encoders follow the general form of equation 4.9 where $H_{NS}(z)$ is the noise shaping filter.

$$Y(z) = S(z) + H_{NS}(z)\ Q(z) \qquad 4.9$$

The transfer function of $H_{NS}(z)$ should have a high-pass response so removing the in-band noise produced by the quantizer. In Chapter 3 equation 3.14, which represented the operation of a d.s.m. in the z-domain, has the same form as equation 4.9, where $H_{NS}(z) = 1 - z^{-1}$, which represents a differentiator which has a high-pass response. This indicates that d.s.m. is a noise shaping encoder. By comparing equation 4.9 with equation 4.1 it

is possible to evaluate the constraints on C(z) and B(z), these are:-

$$B(z) = \frac{1}{H_{NS}(z)} \qquad 4.10$$

$$C(z) = (1 - H_{NS}(z)) \qquad 4.11$$

$$H_{NS}(z) = \frac{1}{1 + B(z)\ C(z)} \qquad 4.12$$

The significant feature of the noise shaping encoder becomes apparent when the decoding filter (D(z)) is considered. Substituting for C(z); from equation 4.11 and B(z) from equation 4.10 into equation 4.3, gives the transfer function of D(z) as:-

$$D(z) = 1 \qquad 4.13$$

This result is possible because of the selection of B(z) and C(z). Thus noise shaping encoders are suitable for generating an intermediate digital code which can be simply converted into an analogue signal by low-pass filtering to remove the out-of-band quantization noise product contained in Y(z).

4.1.4 Optimizing the Noise Shaping Filter

The noise shaping filter is assumed to be an F.I.R. filter with the general form:-

$$H_{NS}(z) = 1 - \sum_{m=1}^{m=N} a_m\ z^{-m} \qquad 4.14$$

The optimum coefficients must be chosen to reduce the in-band coding noise, produced by the quantizer, appearing at the coder's output to a minimum.

The work by Tewksbury and Hallock gives two approaches for optimizing the filter coefficients (a_m). One method to minimize the in-band coding noise power (P_N) involves solving N simultaneous equations of the form $\partial P_N / \partial a_m = 0$. Such a technique results in an optimal design which

assumes that the quantization errors are random. The coefficients obtained depend on the sample rate, but converge at high sample rates towards constant integer values (Ref. 4.1).

The second technique involves expanding the mean square in-band encoding noise (P_N) as a power series and choosing the coefficients, a_m, such that the first N terms of this expansion tend to zero. The optimum form of filter using this technique was shown to be:-

$$H_{NS}(z) = (1 - z^{-1})^N \qquad 4.15$$

At high sample rates these two methods yield identical results.

4.2.1 Theoretical Performance

It is possible to calculate the reduction of in-band noise achieved by using a particular filter ($H_{NS}(z)$). Similar results obtained by Tewksbury and Hallock suggested that the in-band noise produced by the quantizer can be reduced by 36 dB if the order of the system is increased from 1 to 2. The d.d.s.m.s previously used is a first order noise shaping encoders, where the filter ($H_{NS}(z)$) has the form of equation 4.15 with N = 1. This is a simple high-pass filter, so significant in-band noise will remain. By using a higher coder filter it is possible to remove more of the in-band noise. The order of the noise filter can be increased indefinitely, but the power of the noise removed will become proportionally less. The order of filter used will be a compromise between the noise reduction achieved and the added complexity required to implement the filter.

Although it is possible to calculate the reduction in noise appearing in the message band due to a particular filter before this can be done it is necessary to make an assumption about the noise spectrum produced by the quantizer. This spectrum is usually approximated as having a uniform power spectral density (Ref. 4.1, 4.2). A similar approximation was made in the analysis carried out in Chapter 3, where it was found only

to be true for high signal input levels. At low signal levels the noise spectrum changes, and contains more power at low frequencies. This shift in the spectrum will reduce the effectiveness of the noise-shaping principle.

The noise spectrum is assumed uniform in the following analysis to enable the high signal level performance of higher order systems to be evaluated. If this improvement is sufficiently large at high signal levels then the noise produced by the noise shaping coder will be below the noise contained in the input signal. If this difference can be made sufficiently large then the reduction in improvement which occurs at low signal levels will not affect the overall system's performance.

The total noise power produced by the modulator will be contained in the band 0 - $f_m/2$. The output of the modulator is either +V or 0, so the total noise power (P_T) is $V^2/2$. An arrangement where the noise spectrum is uniform is shown in Figure 4.2a; this approximates that produced by the quantizer in Figure 4.1. The total power can then be expressed:-

$$P_T = \int_0^{f_m} Q(f)\, df = \frac{V^2}{2} \qquad 4.16$$

$Q(f)$ = quantizing noise spectral density

According to equation 4.9 this spectrum is changed by the action of the noise shaping filter, but the total power up to $f_m/2$ will still equal P_T. This is illustrated in Figure 4.2b-d, which shows the noise power spectrums (Np(f)) produced by first, second, and third order systems. If the decoder consists of an ideal low-pass filter then only the noise contained in the message band (B = 0 -f_s) will appear in the decoded output signal.

It is possible to obtain an expression for the power spectral density function of the noise signal. Defining $|H_{NS}(f)|^2$ as the power transfer function of the noise filter, the total noise power is given by:-

$$P_T = K \int_0^{\frac{f_m}{2}} |H_{NS}(f)|^2\, df = \frac{V^2}{2} \qquad 4.17$$

K = constant

Since the value of P_T is known it is possible to evaluate the constant K, for each filter ($H_{NS}(z)$). The total in-band noise power (P_s) is then given by:-

$$P_s = K \int_0^{f_s} |H_{NS}(f)|^2 \, df \qquad 4.18$$

Since K is known from equation 4.17, P_s can be evaluated. The maximum signal power that the encoder can output will be $V^2/2$. The maximum signal to noise power can now be calculated and these results are summarised in the table below:-

Order of $H_{NS}(z)$	Peak Signal to Noise Power
1	-60.95 dB
2	-100.24 dB
3	-136.3 dB

Results of evaluating equation 4.18 at:

f_m = 4096 KHz

f_s = 16 KHz

These results indicate that a second order system would introduce insignificant additional noise when encoding a 14-bit P.C.M. signal.

4.2.2. Development of a Second Order System

The results of the analysis described in section 4.1 gave the noise shaping filter in a second order system as:-

$$H_{NS}(z) = (1 - z^{-1})^2 = 1 - 2z^{-1} + z^{-2} \qquad 4.19$$

The transfer functions of the feedforward filter (B(z)) and feedback filter (C(z)) can be calculated from equations 4.10 and 4.11 as:-

$$B(z) = \frac{1}{(1-z^{-1})^2} = \frac{1}{1 - 2z^{-1} + z^{-2}} \qquad 4.20$$

$$C(z) = 1 - (1-z^{-1})^2 = 2z^{-1} - z^{-2} \qquad 4.21$$

A second order system, suitable for D/A conversion of 14-bit P.C.M. can be realised using the components configured in Figure 4.3. It is possible to take advantage of the single bit output of the system and simplify the implementation of the feedback filter (C(z)). This is possible because there are only four distinct values for the output of this filter, which can be obtained using combinational logic. The simplified arrangement is shown in Figure 4.4. To ensure that this system performed satisfactorily and to verify the results calculated in the previous section a simulation of the system was undertaken.

4.2.3 The Simulation System

A series of software packages were written to enable the stability and performance of the proposed system to be assessed. The general form of the simulation system is shown in Figure 4.5. It consists of a main program which controls a number of subroutines. Details of the programs are presented in Appendix 4. The main part of the program allows the required user options to be selected. These include, the required input signal frequency, amplitude and initial conditions. It also controls the order in which the subroutines are called. The first subroutine (DATA) produces an array of samples which form the input to the second order modulator (SDSM). A single cycle of data is produced. This data is sampled and quantized to represent a 14-bit P.C.M. signal, sampled at 32 KHz, to reduce the amount of samples required the input data is restricted to sinusoidal signals whose frequencies are at submultiples of the sample rate.

The second order system is simulated in the subroutine (SDSM). Its operation closely follows the functional diagram given in Figure 4.4.

Extensive use is made of integer arithmetic to simulate the quantization found in the equivalent hardware. The structure of this subroutine is flexible to enable the effects of different starting conditions to be investigated. The magnitude of the numbers used at various points in the simulation is monitored. The results on the maximum values obtained during operation permit the equivalent hardware to be designed to avoid any intermediate numbers overflowing. An array stores all the output representing a complete cycle of input data as a series of +1 or -1 integers.

The output of the simulated system is applied to a Fourier transform subroutine (FFT). This enables measurements on the noise produced by the coder to be made. The output produced by DATA is also applied to the FFT. This permits comparisons on the noise produced by the quantizing of the input signal, to the noise introduced by the encoder. As both sets of data contain a full cycle of respective periodic signals the FFT can be taken directly. This is equivalent to using a rectangular window on the data in the time-domain. Consequently the transformed data is convolved with a Sin x/x function which is the transform of the rectangular window. Since the input data to the FFT is periodic its frequency spectrum will consist of a line spectrum. The zeros of the transformed window will lie on the line spectrum of the input data, and if the FFT is only evaluated at these points the windowing of the data will not effect the output spectrum required. Thus, using a periodic set of data enables the complexity of the FFT to be kept low.

It is then possible to compare the power contained in the input signal's and output signal's harmonics. Also the power contained in the fundamental can be compared with the total power contained in the remaining in-band harmonics to give an indication of the system's signal to noise ratio.

Although the output signal produced by the simulated system represents a complete cycle (block) of input data, continuation of the

simulation over further cycles has shown that each block of the modulators output is different. The FFTs of these "blocks" of data are also slightly different. Since no discontinuity between adjacent blocks occurs the differences must arise because there is more than one sequence of data which can represent a complete cycle of input data. The particular sequence of data outputed by the encoder depends on the initial conditions within the encoder at the start of each cycle. These conditions depend on the residual numbers left in the accumulators at the end of the previous cycle. In a practical system the measurements of signal to noise ratio and harmonic distortion would be taken over many cycles of data so any variations would be averaged out.

To make the simulation more realistic it would be necessary to increase the size of the FFT to include many cycles of input data. As this would increase the complexity and computation time of the simulation an experiment was carried out to assess the size of this variation. These results are summarised in Figure 4.6. Taking the FFT of many blocks of data indicates that only a slight variation in the overall signal to noise ratio occurred. Therefore, since a practical system was to be constructed it was considered acceptable to continue the simulations by only taking the FFT of one block of data.

A graph showing the signal to noise ratio as a function of input signal level of the simulated input data and the coders output is given in Figure 4.7. These results indicate that a second order system is capable of accurately encoding 14-bit input data, when clocked at 4 MHz.

It was found in the simulation that the encoder became unstable when very large input signals were applied. The range of input signal levels causing instability was from peak input (0 dB) to -0.5 dB. This instability is due to the feedback loop saturating at high input signal levels.

4.2.4 Modifications to the Second Order System

Instability was also observed in a second order system described by Petit and Mactre (Ref. 4.3). Their solution was to change the coefficients in the feedback filter (C(z)) according to equation 4.21 where:-

$$C(z)' = 4\,z^{-1} - 2\,z^{-2} = 2C(z) \qquad 4.21$$

The effect on the input/output transfer characteristic can be investigated by substituting for C'(z) and B(z) into equation 4.1 this gives the result:-

$$Y(z) = \frac{S(z)}{1 + 2z^{-1} - z^{-2}} + Q(z).\frac{1 - 2z^{-1} + z^{-2}}{1 + 2z^{-1} - z^{-2}} \qquad 4.22$$

This expression is no longer in the form of equation 4.9 a noise shaping encoder, however, arranging it in a convenient form to obtain:-

$$Y(z) = S(z).H_s(z) + Q(z).H_{ns}'(z) \qquad 4.23$$

where:-

$$H_s(z) = \frac{1}{1 + 2z^{-1} - z^{-2}} \qquad 4.24$$

$$H_{ns}'(z) = \frac{1 - 2z^{-1} + z^{-2}}{1 + 2z^{-1} - z^{-2}} = H_{ns}(z).H_s(z) \qquad 4.25$$

To enable this modified system to function as a noise shaping encoder which can be used with the existing decoder, the new filter $H_s(z)$ must introduce no in-band attenuation. If $H_s(z)$ is a low-pass filter whose cut off frequency is outside the messages band, then equation 4.23 simplifies to equation 4.1. Less noise is removed from the message band with this modified noise filter ($H_{ns}'(z)$) since its frequency response has been modified by the action of $H_s(z)$. Repeating the analysis given in Section

4.2.1 the performance of the modified system can be estimated, yielding the following results;-

Order of $H_{NS}(z)$	Calculated Peak Signal to Noise Power
Second	-100.24 dB
Modified second	-98.9 dB

These results show that the modified filter has little effect on the overall system performance. An undesirable aspect of changing the filter coefficients can be seen if the frequency response of the input filter ($H_s(z)$) is considered.

$$H_s(f) = \frac{1}{2(1 + \sin^2(2\pi fT))} \qquad 4.26$$

This shows that the filter attenuates all frequencies by two. With reference to equation 4.23 the filter will reduce the maximum output produced by the coder by a factor of two. This means that only half the possible range of output codes will be used by the coder. Consequently the demands on the noise performance of the output circuitry, where the D.S.M. output is filtered to produce an analogue output, is increased. This solution appears rather pointless, because the instability problem only occurs at input signals approaching peak level and simply reducing the input signal by half would remove the problem.

The results of simulating the modified system are shown in Figure 4.8 and compared with the original system, the slight reduction in performance due to the modified noise filter can be seen.

Two other methods of avoiding the instability are investigated in this section. The simplest involves limiting the range of input signals to below the point where instability occurs. This means reducing the

dynamic range of the coder slightly. Since the reduction required is only 0.3 dB in a total range of 84 dB it is considered insignificant. The reduction can be ensured by placing a hard limiter at the input to the coder.

An investigation into removing the instability occurring in the encoder by changing the coefficients of the filters was undertaken. There is little practical value in finding a solution by changing the coefficients of B(z), since the hardware required to accomplish any change would be uneconomic. The output of C(z) has only four possible values so modifications can be simply implemented. Simulations have shown that a stable system can be achieved if C(z) is modified according to:-

$$C(z) = 2{,}25\ z^{-1} - z^{-2} \qquad 4.27$$

This arrangement prevents the encoder latching up, but reduces the signal to noise ratio at peak signal levels to only -55 dB. Simulated results of these systems are given in Figure 4.9.

In conclusion this section has shown that a second order system can be built and is capable of achieving 14-bit P.C.M. performance. Instability has been shown to occur at high input signal levels, but three methods of removing the problem have been suggested.

4.3.1 A Practical Second Order System

In view of the simulated and calculated results a second order system was designed and constructed. The hardware design is shown in Figure 4.10. The configuration of the feedforward filter (B(z)) is illustrated, consisting of two sets of 20-bit adders and two 20-bit buffers. The feedback filter consists of two inverter gates which feed the M.S.B. of the buffers back to the input of B(z). A full explanation of this circuit is given in Appendix 3. The use of standard L.S. series TTL M.S.I. logic circuits enables circuit operation up to 6 MHz without the need of additional look-ahead logic. Various versions of this hardware were built

to enable the different feedback filters (C(z)) to be tried.

The analogue circuit described in Section 2.2.5 can be used to eliminate the effect of unequal rise and fall times in the output signal.

It is possible to convert the circuit to encode higher input sample rates by clocking the existing input buffer stage at the new sample rate.

There are no complex elements in this design so it could be simply integrated on a single L.S.I. integrated circuit.

4.3.2 Performance of the Practical System

The circuit was tested in its original form, and found to perform in the predicted manner. The instability which was predicted, only occurred on very large signal peaks and the system recovered as soon as these large signals were removed. When the limiting circuit was added, operation was stable over all signal levels and frequencies.

The measurements of signal to noise over the entire input signal range indicated that full 14-bit P.C.M. performance had been obtained. The signal to noise characteristic is shown in Figure 4.11a

The harmonic distortion and level of all the inband harmonics produced by the coder are at a very low-level. The spectrum of a high-level input signal of 500 Hz is reproduced in Figure 4.12a.

One deviation from the predicted results was found to occur at high frequency peak input signals when the level of the second harmonic increased. This rise was attributed to slewing in the operational amplifier in the differential amplifier of the output circuit. This indicates that particular care must be taken to ensure any further prototypes are produced with a high performance amplifier. This would be the limiting factor in a mass produced product.

The quantity of reproduction using the tests discussed in Appendix

2 confirmed the high accuracy of the system and absence of background noise.

The modified version of C(z) suggested by Petit and Maitre was also tested. This was found to perform in a similar manner, although the results obtained were slightly inferior. A comparable plot of the signal to noise ratios is given in Figure 4.11b. Additional problems were encountered because the peak output of this system was half the normal level, this increased the effective noise floor of the output circuits and measuring equipment by 6 dB. As a result additional compensation had to be introduced to remove clock noise on the output of the operational amplifier.

Again this indicates the limitations of the remaining analogue components of the D/A. A spectrum of the harmonic distortion is given in Figure 4.12b.

The results of modifying the coefficients of C(z) according to Equation 4.27 revealed that instabilities in the feedback loop still occurred although at a reduced level. Observations of a sinusoidal peak level signal showed a small burst of instability on approximately one cycle peak in five. Further experiments failed to produce a stable system by this method.

A comparison of the level of individual harmonics produced by the coders when a pure sinusoidal input signal is applied is shown in the following table:-

Harmonic Number	Level Using 2nd Order System	Level Using Modified Second Order	Level of Reference D/A Converter
1	0 dB	0 dB	0 dB
2	-88 dB	-87 dB	-90 dB
3	-85 dB	-83 dB	-80 dB
4	-98 dB	-92 dB	-
5	-95 dB	-	-
Total Harmonic Distortion	0.0072%	0.0073%	0.01%

Noise floor of Instruments -100 dB

4.3.3 Higher Order Systems

The previous section has shown how an optimal second order system performs. It is possible to further increase the amount of noise removed from the message band by increasing the order of the noise filter. In section 4.2.1 the theoretical performance of a third order system was given. These results predict an improvement in peak signal-to-noise ratio, of 76 dB, over a first order system. Such a system would enable the clocking frequency of the encoder to be reduced, but still permit the required performance to be obtained. The structure of a third order system can be calculated in an identical manner to the second order system, the results obtained show:-

$$H_{NS}(z) = (1 - z^{-1})^3 \qquad 4.28$$

$$C(z) = 3z^{-1} - 3z^{-2} + z^{-3} \qquad 4.29$$

$$B(z) = {}^{1}/_{(1 - 3z^{-1} + 3z^{-2} - z^{-3})} \qquad 4.30$$

A block diagram of a third order system is given in Figure 4.13. The increase in complexity of this system, particularly in the feedforward filter B(z) make it less attractive than the second order encoder. The multiplication required would best be spread over two stages using a shift and add technique. Investigations using a simulated third order encoder, highlighted severe instability in the feedback loop. Various techniques were tried to achieve a stable system, but none proved satisfactory. Unstable operation did not occur in a third order system using a multi-bit quantizer.

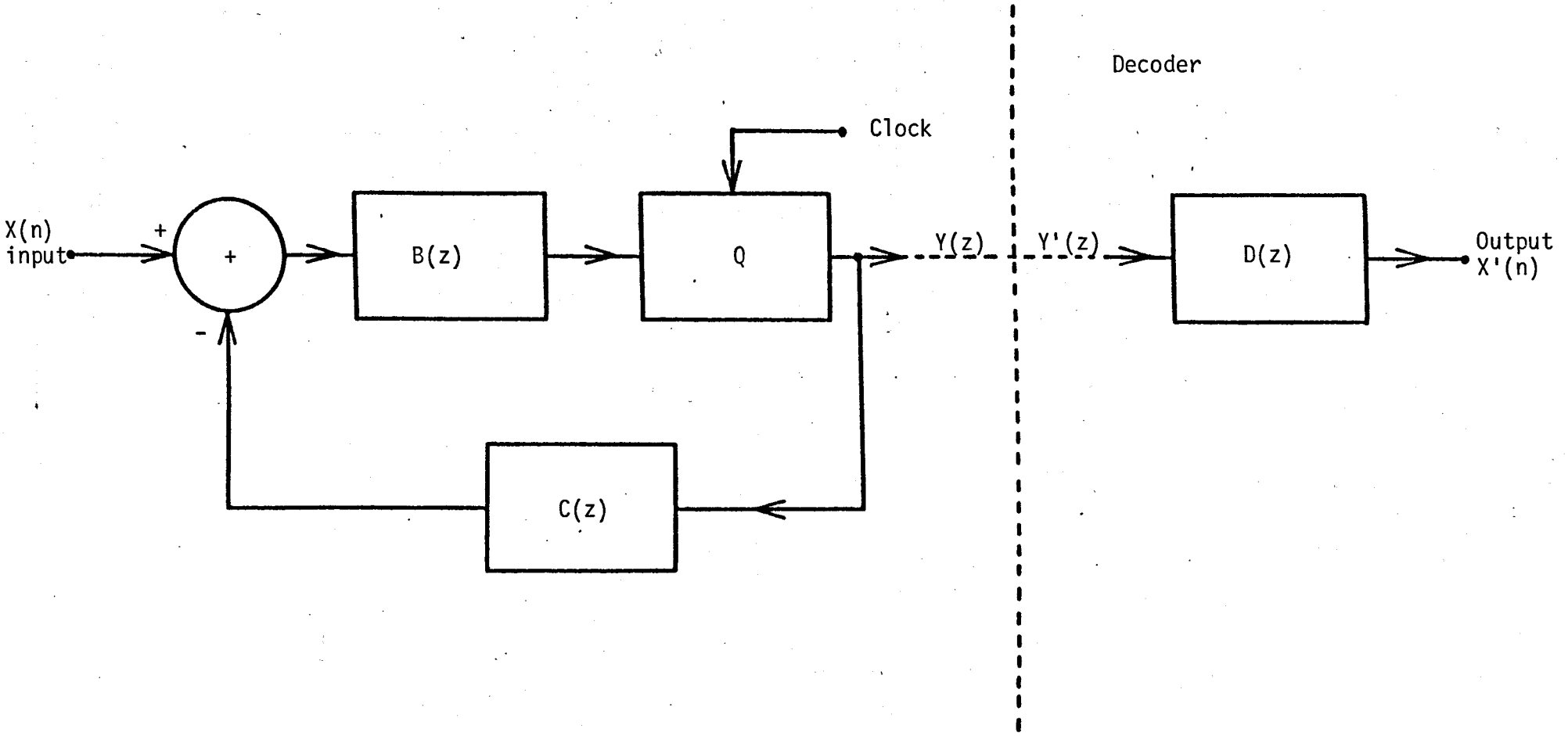
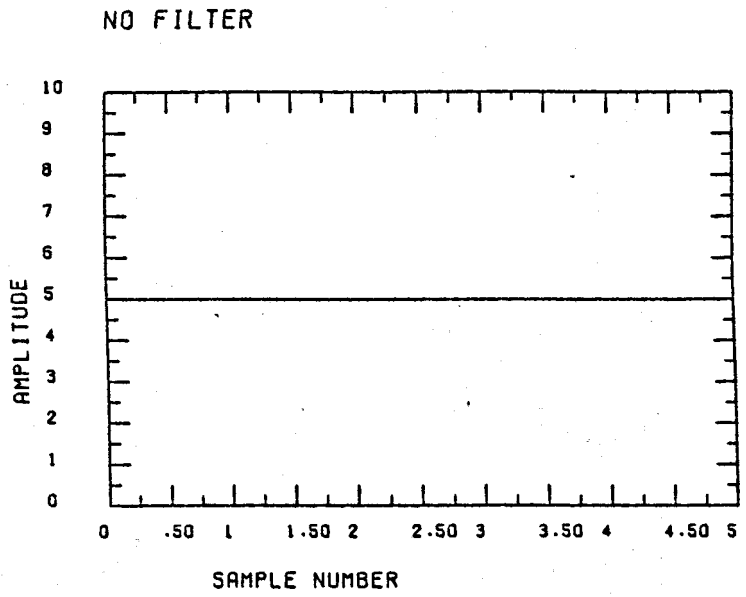
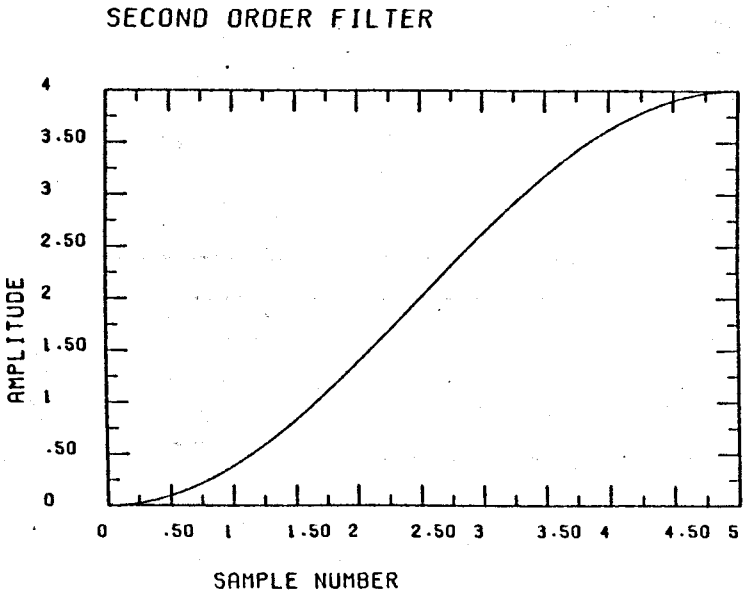
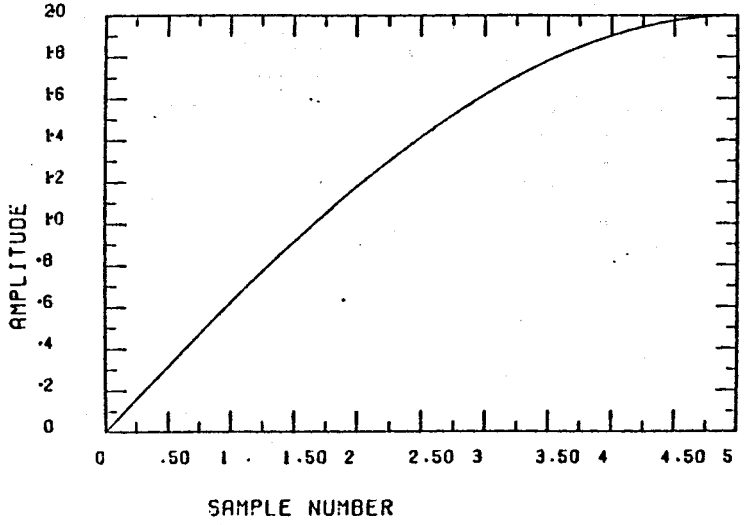


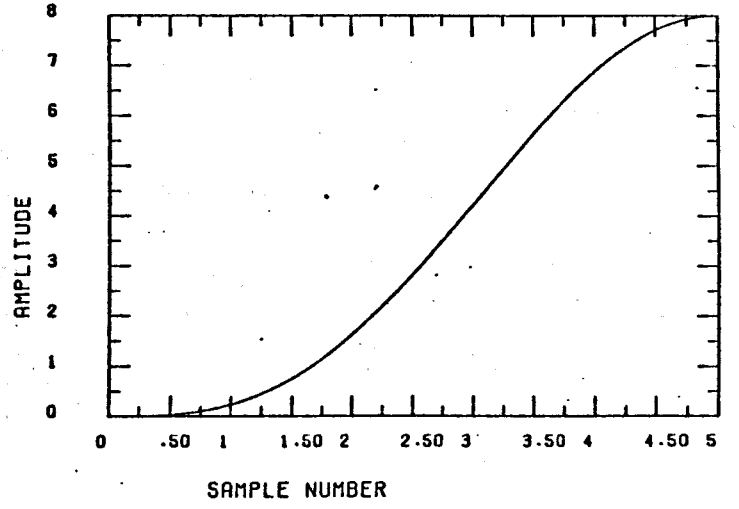
Figure 4.1 A general linear feedback system.

Figure 4.2 *Response of noise shaping filters.*









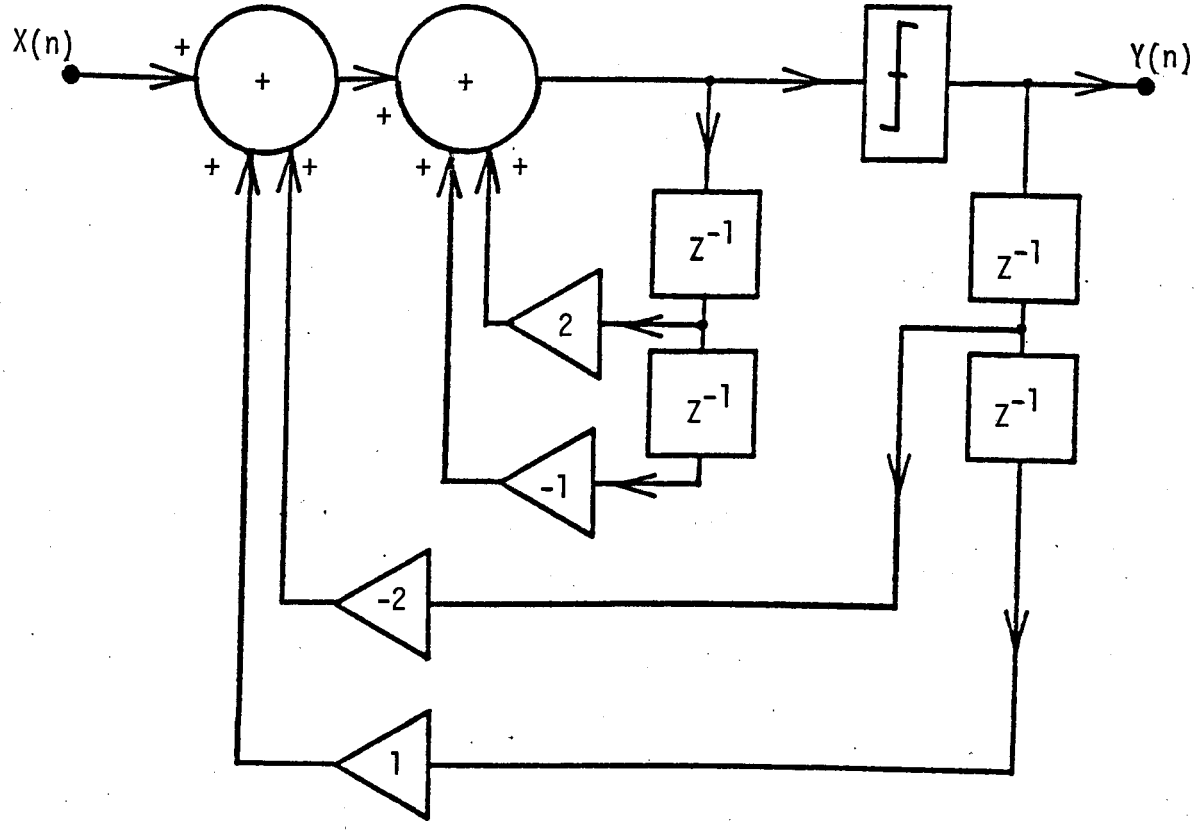


Figure 4.3 Second order noise shaping encoder.

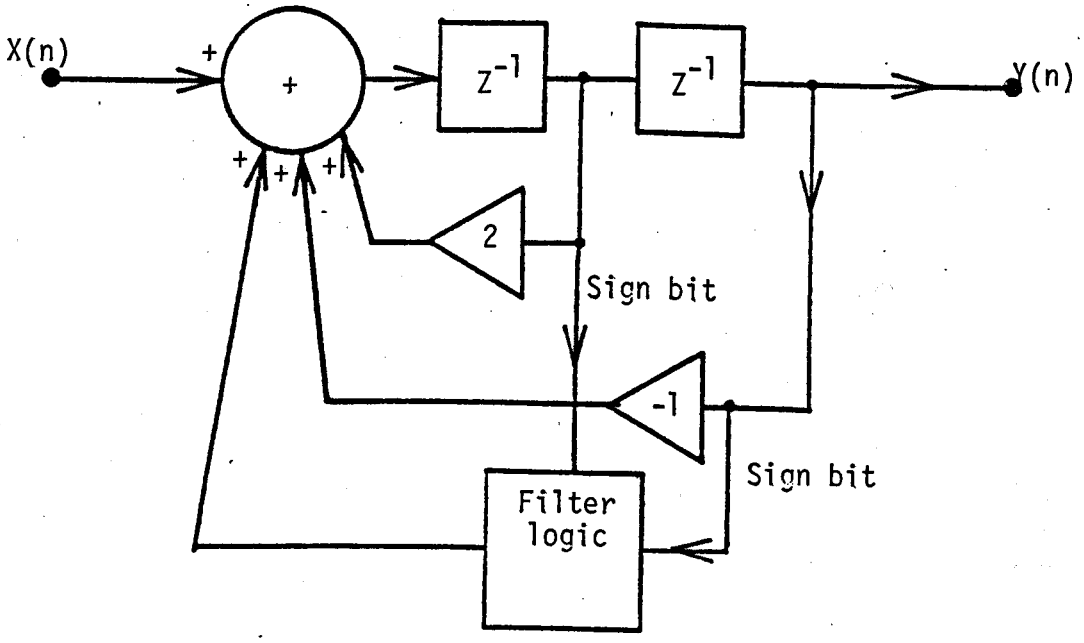


Figure 4.4 Simplified second order system.

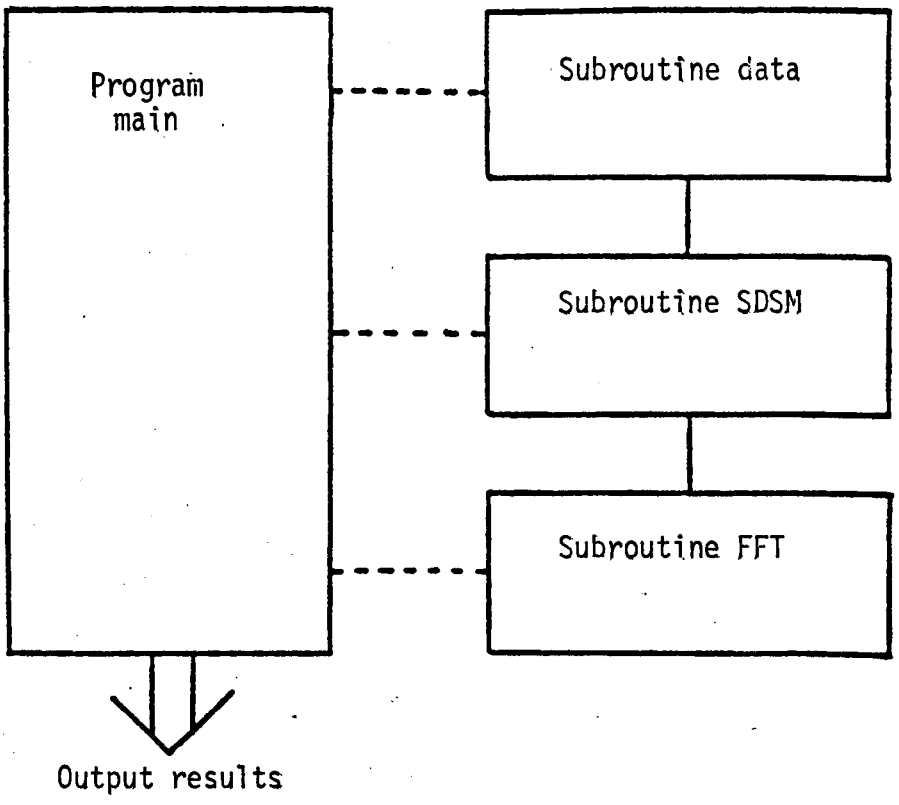


Figure 4.5 The layout of the modulator's simulation program.

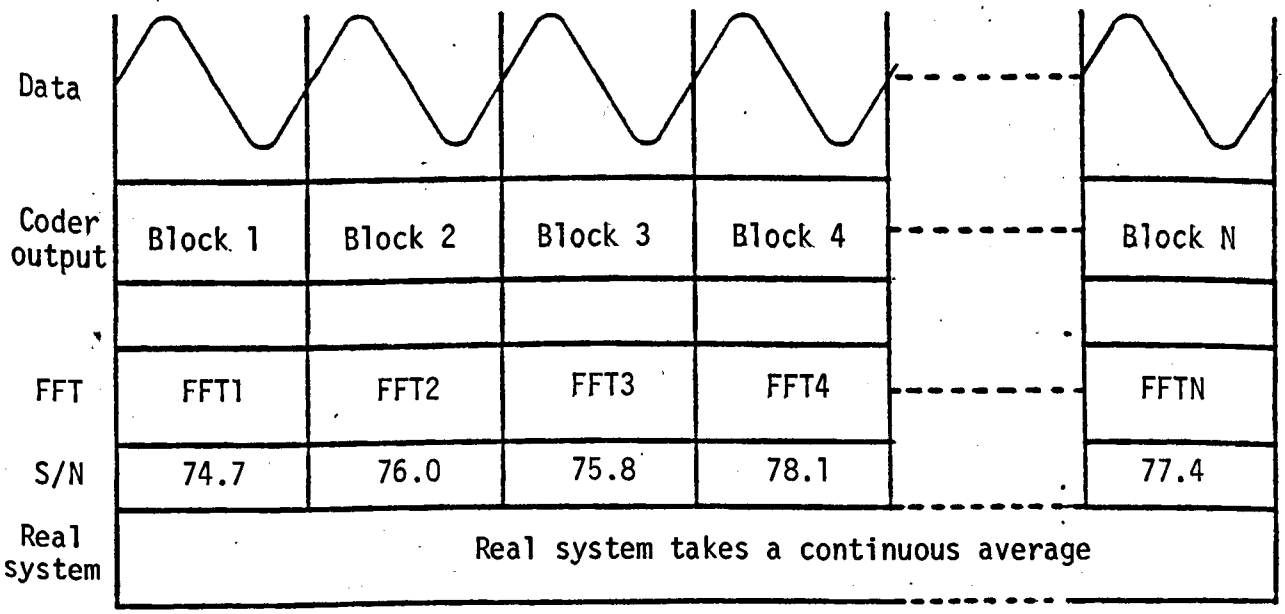


Figure 4.6 Summary of the results obtained using the simulation program to process blocks of data.

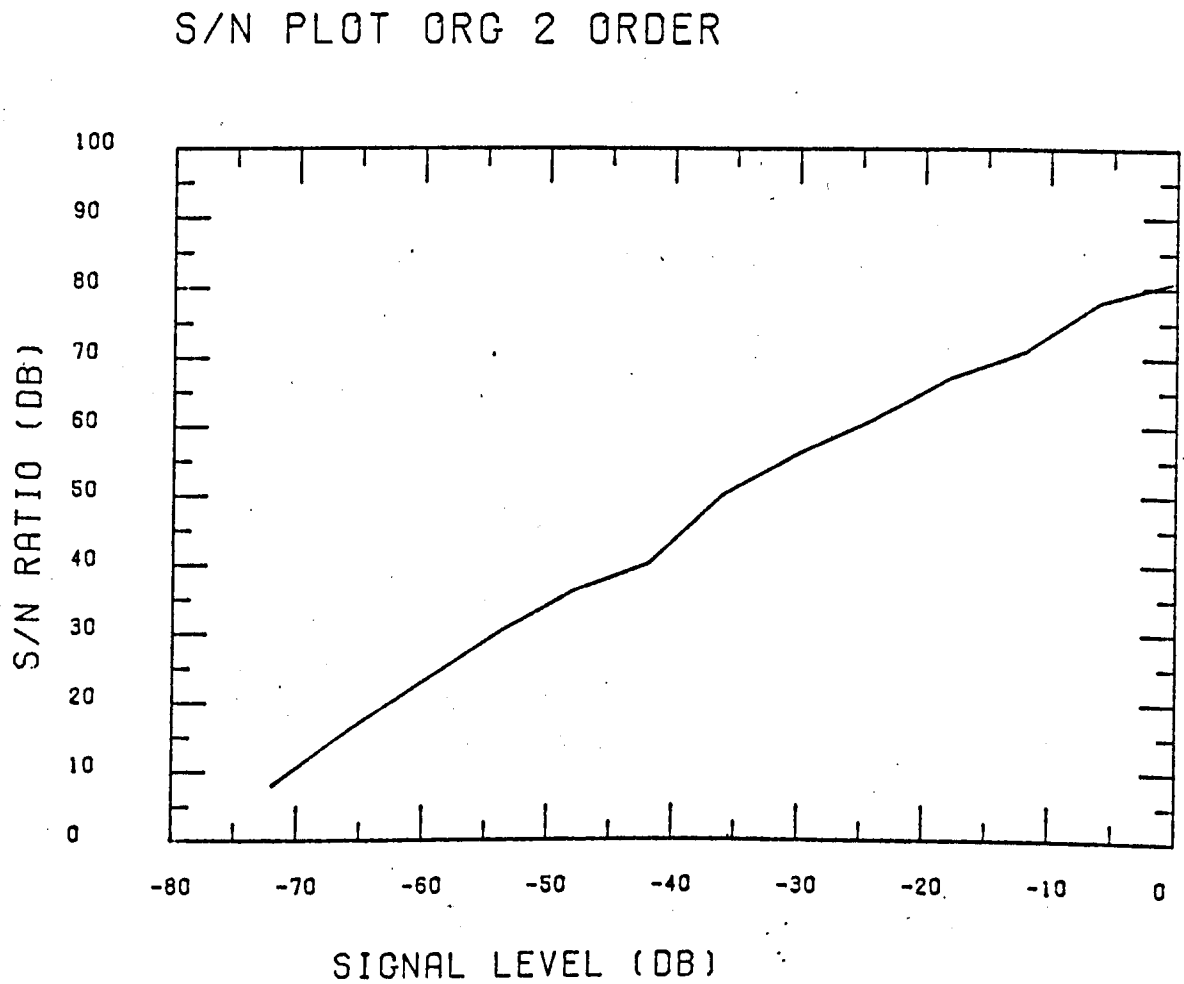


Figure 4.7 Simulation results of 2nd order system.

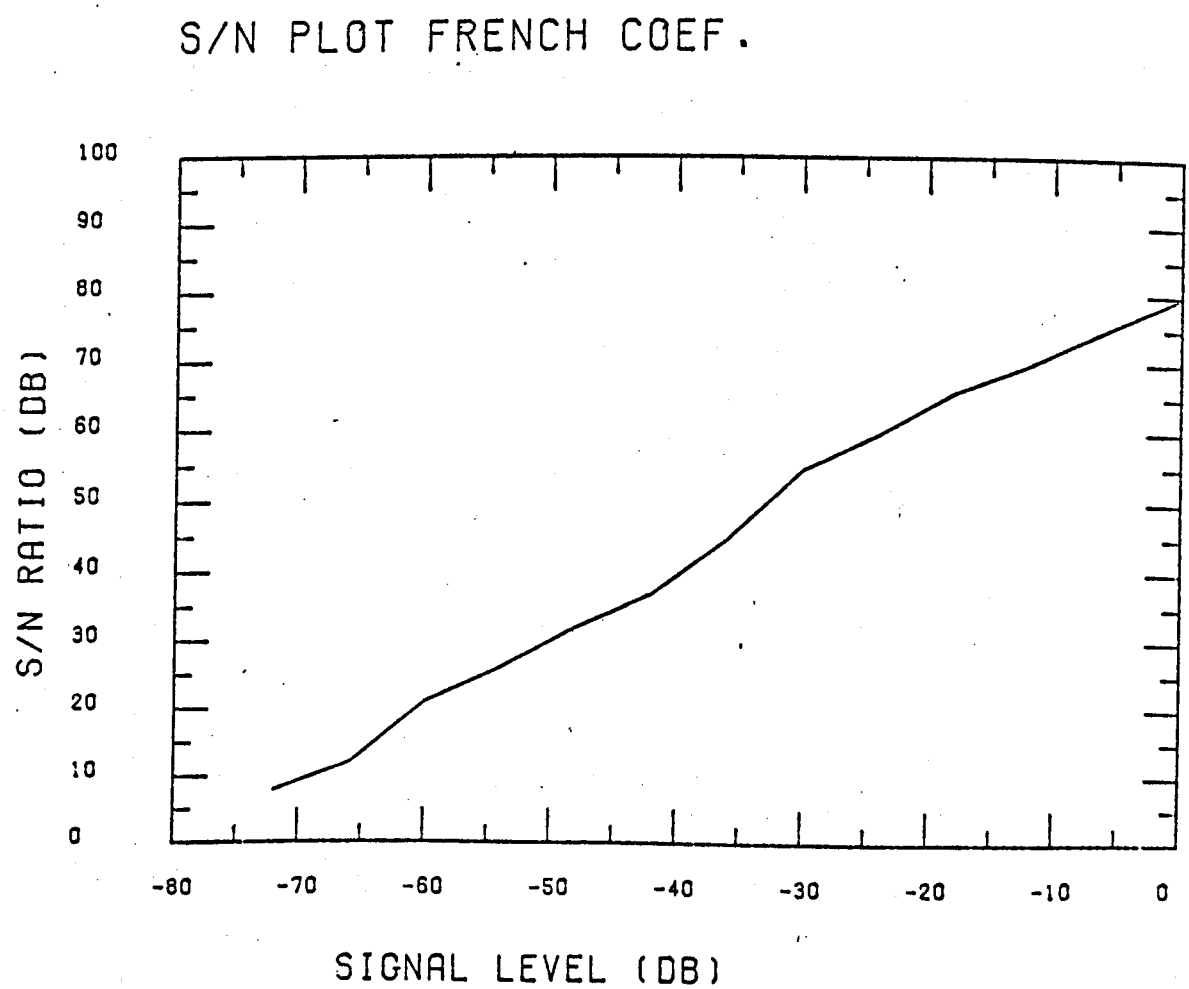


Figure 4.8 Simulation results of modified 2nd order system.

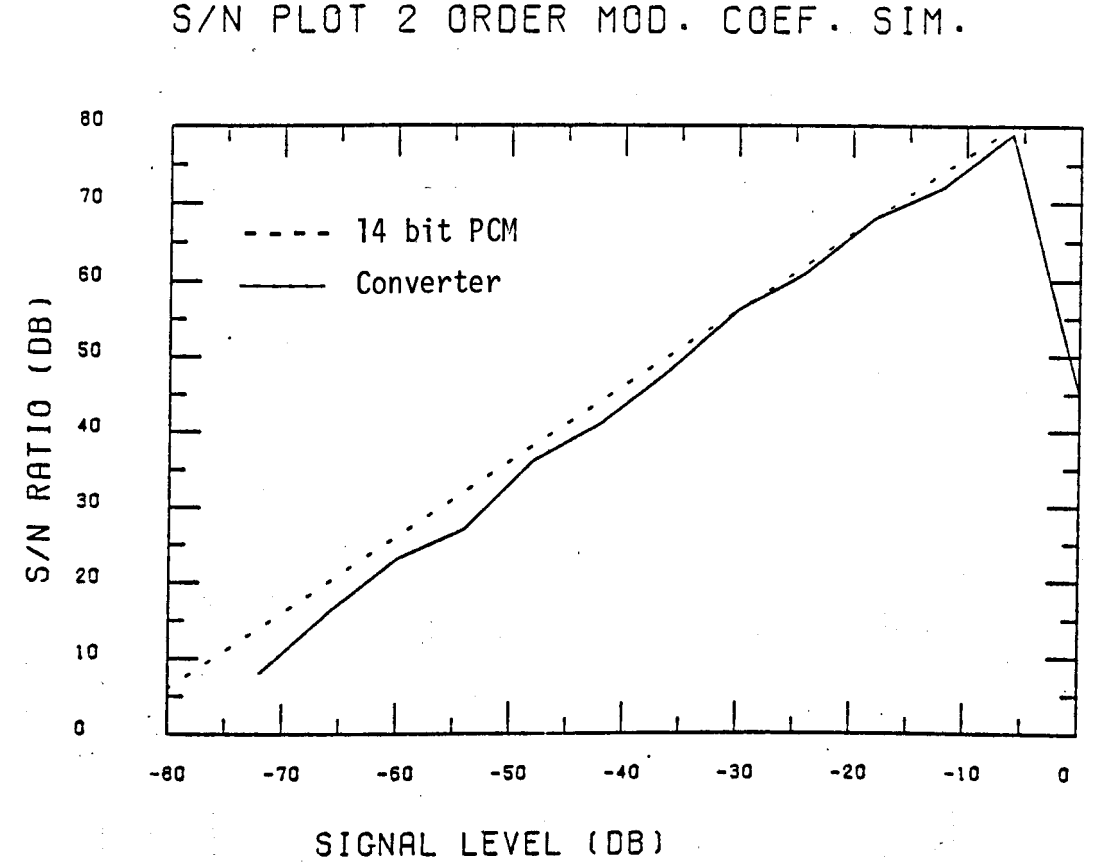


Figure 4.9a Results of modifying the 2nd order D.S.M. coefficient.

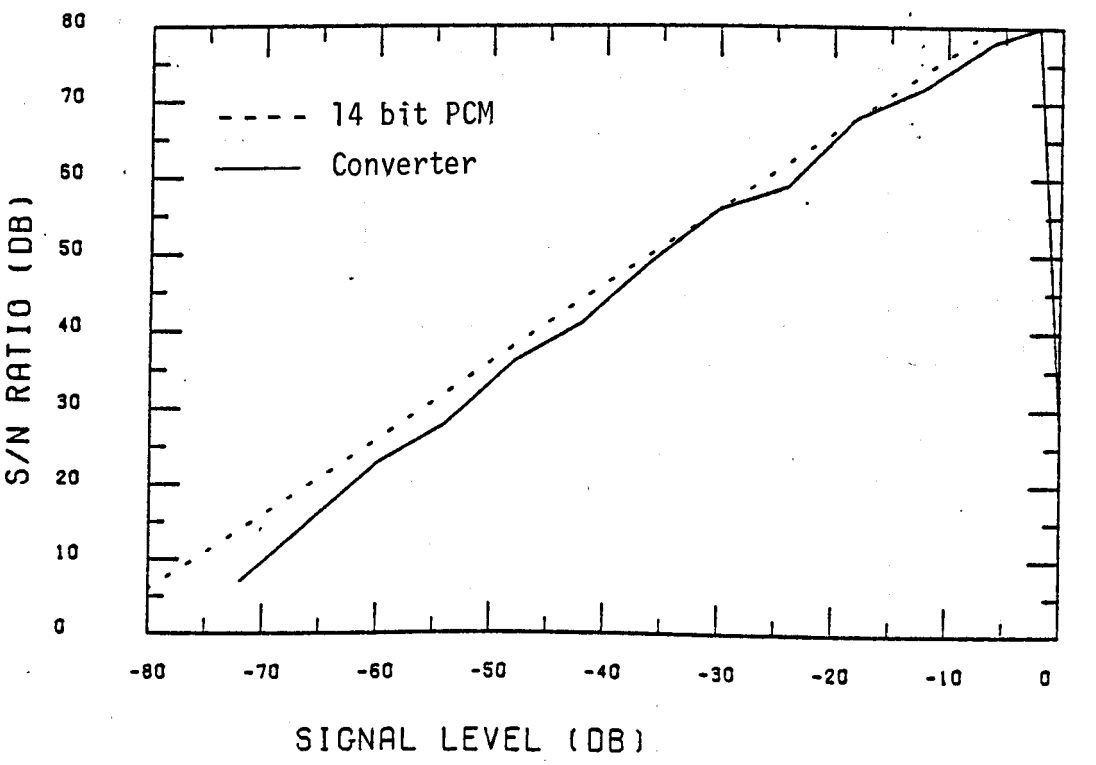
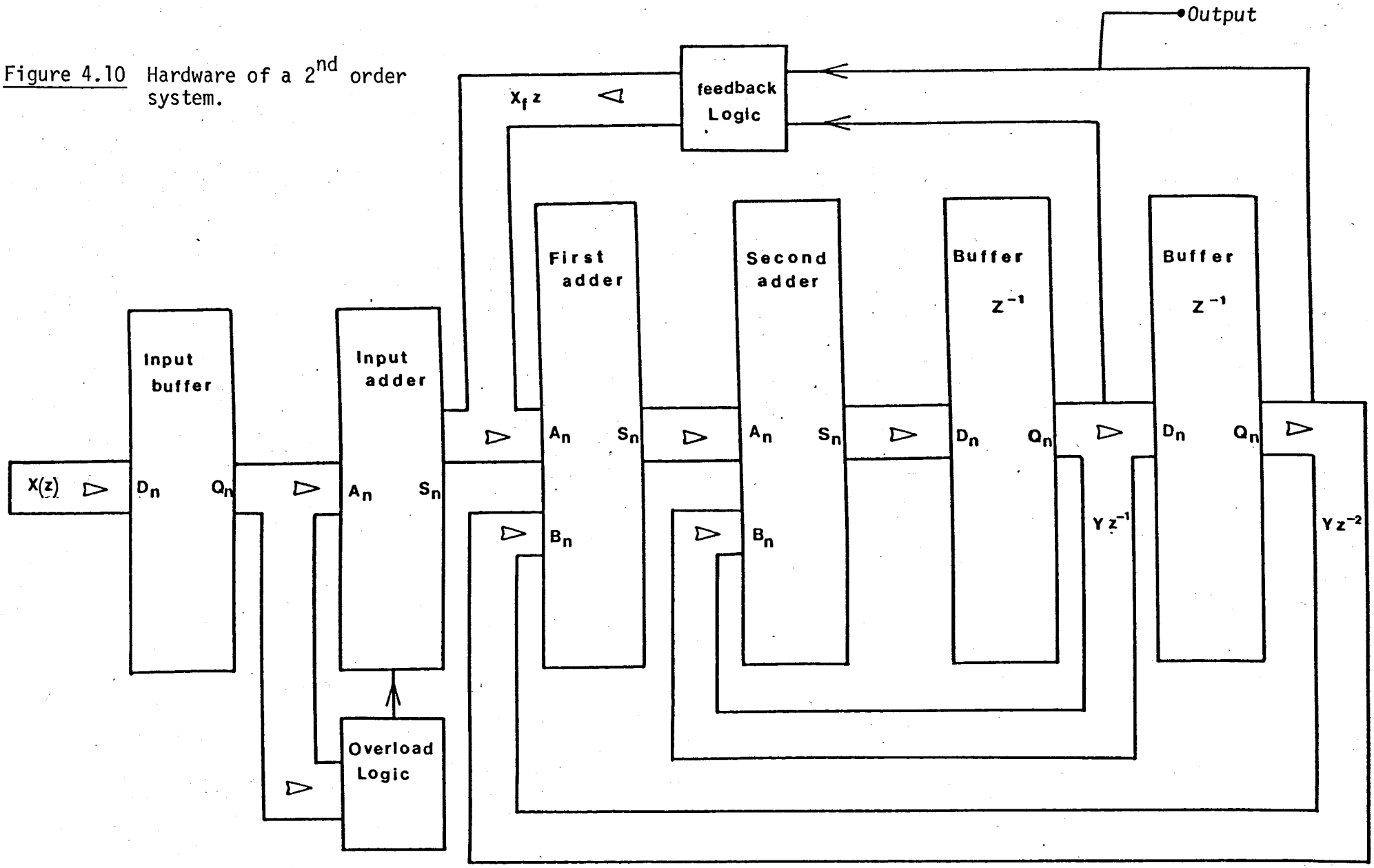


Figure 4.9b Results of limiting input range.

Figure 4.10 Hardware of a 2nd order system.



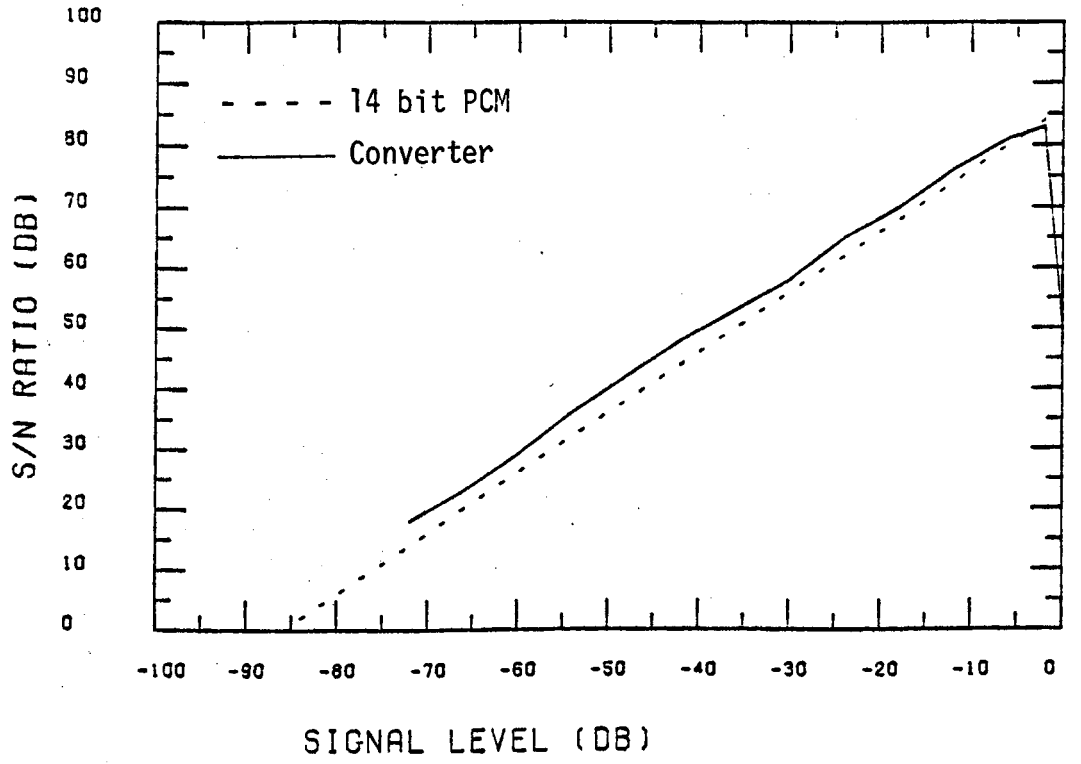


Figure 4.11a Noise performance of 2nd order D.S.M.

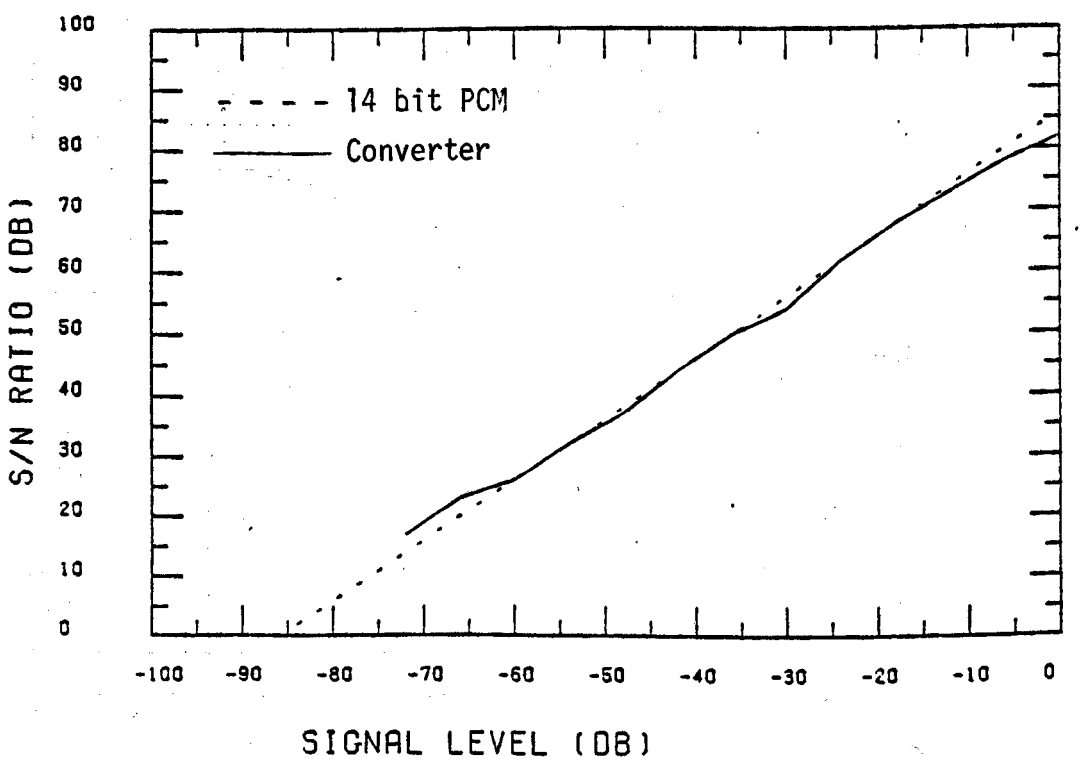
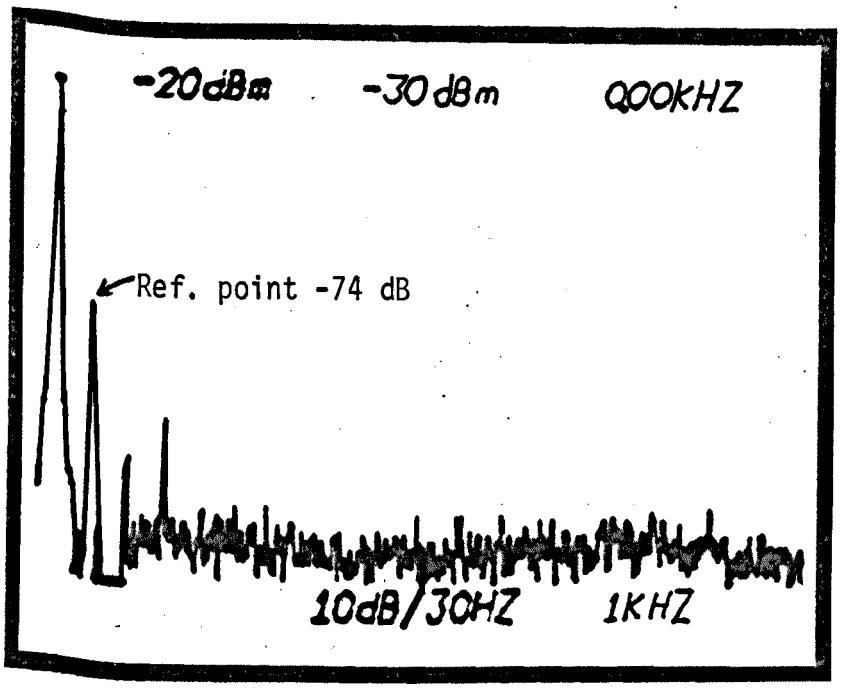


Figure 4.11b Noise performance of modified 2nd order D.S.M.

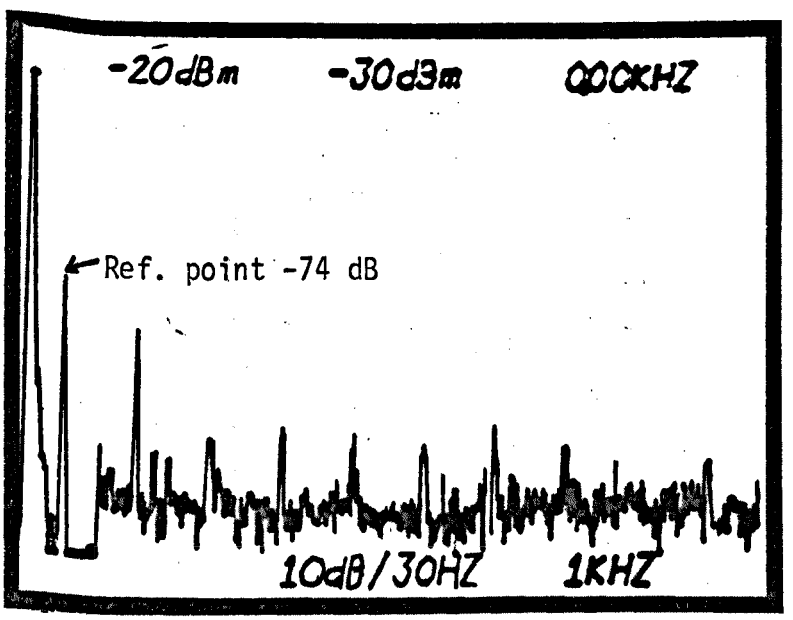


Vert. scale
10 dB/0.8 cm

Horiz. scale
1 kHz/0.8 cm

Bandwidth
30 Hz

Figure 4.12a Spectrum of a 500 Hz signal encoded by a 2nd order D.S.M.



Vert. scale
10 dB/0.8 cm

Horiz. scale
1 kHz/0.8 cm

Bandwidth
30 Hz

Figure 4.12b Spectrum of a 500 Hz signal encoded by the modified 2nd order D.S.M.

Harmonic No.	2nd order system	Modified 2nd order
Fund.	- 6 dB	- 6 dB
2nd	-98 dB	-
3rd	-90 dB	-79 dB
4th	-	-

Comparison of the harmonic levels of the two types of D.S.M.

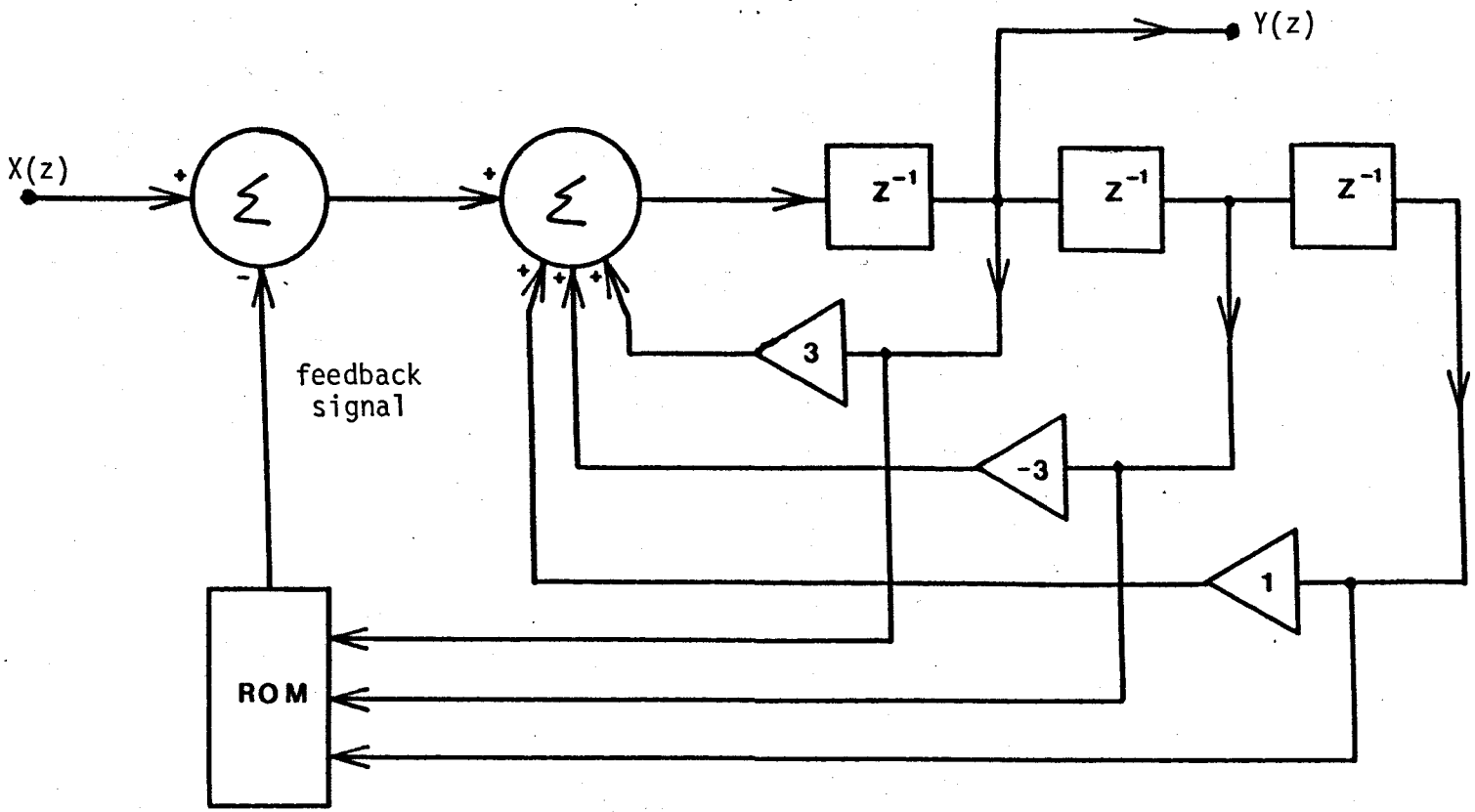


Figure 4.13 Proposed third order system

CHAPTER 5

DIGITAL AUDIO SYSTEMS AND DIGITAL POWER AMPLIFIERS

The previous chapters have described the development of D/A converters suitable for high quality audio signals. These converters only form part of the complete system which is necessary to produce high quality audio. The summary at the end of Chapter 1 described how digital audio equipment could be introduced alongside existing analogue audio systems. It was further suggested that digital systems could eventually replace all the analogue hardware required, except the power amplifier. The first section of this chapter briefly describes how the user controls, such as tone filters, can be implemented digitally. The second section of the chapter describes the construction of an all-digital class D power amplifier which is particularly suited for use with D/A converters employing code converters.

5.1.1 The Control of Audio Systems Using Digital Hardware

It is necessary to consider what facilities need to be under user-control in an audio system before the requirements of a digital alternative can be investigated. The controls of a typical audio system can be summarised as:-

1. Selection of the required program source
2. Adjustment of the program's amplitude
3. Control of the shape of the system's frequency response.
4. Possible mixing of one program with another

This list only considers the basic requirements of an audio system, the complexity of each item will depend on the required specifications. The

control of these functions in an analogue system requires separate circuitry for each function.

If the user controls are implemented digitally, care must be taken to ensure that no additional distortion or noise is added to the signal. Although digital systems are immune to circuit noise they can still introduce additional noise. This noise is produced by the processing of digital words within the finite range of levels available leading to rounding noise. The following sections describe some of the problems resulting from the digital signal processing of audio signals.

5.1.2 Selection of the Required Program Source

This is perhaps the easiest function to implement in digital form. Since the input signals are in digital form the input selector switch needs to ensure that each output bit is connected as required, to the corresponding input bit. The complexity of this system depends on the number of bits in each digital word (n) and the number of input words available. Such data selectors are common in computer systems where a number of input ports can be connected to a common data bus, each port is activated as required under the control of a central processor or other forms of intelligent hardware. The complexity of such systems is low and since digital information is controlled without any arithmetic operations, no noise is introduced, furthermore the control circuitry can be remote from the switching hardware.

For this system to function satisfactorily all the required input signals must be in the same format. Although it is possible to mix digital signals with different numbers of bits by scaling, all these signals must have the same sampling frequency. Therefore each input must be under the control of a synchronising signal controlled by the D/A sampling frequency. If different sample frequencies are used conversion between them is only possible when digital interpolation filters are used. The complexity of

these circuits is high and currently beyond the scope of a domestic system.

An analogue input channel could be provided by using a suitable A/D converter, its output would then be manipulated in an identical manner to other digital inputs.

5.1.3 Adjustment of the Program Amplitude

There are two main approaches to this requirement. A digital solution can be provided by simply shifting the bit-field between the input and output words this will produce 6 dB increments or decrements in volume. When increasing the signal's amplitude by this method it is necessary to provide a limiter on the output signal to avoid large input signal peaks corrupting the sign bit,so producing an incorrect output word. These 6 dB steps are too coarse for most requirements. To produce finer steps it is necessary to multiply the input data by the required scaling constants. Since this multiplication would have to be accomplished at the sampling frequency a high speed multiplier would be required. The use of a multiplier could be avoided by performing the multiplication using look-up tables. The resolution required then determines the size of the look-up table.

The level of noise produced by a digital system is constant and determined by the number of bits in the code applied to the D/A converter. Changing the output level of the signal by scaling the digital data will not affect this noise and since most systems never operate at full power, the available dynamic range will be reduced. As an example, a 14-bit system has a S/N of 86 dB, if the average volume level was set at -20 dB then the resulting S/N would only be -66 dB, this is comparable with existing analogue equipment.

A variation of the normal analogue gain control can be used with advantage. The adjustment of the program's amplitude can be left until after D/A conversion, then a normal gain control can be employed. This

adjustment would be under the control of a digital signal to ensure compatibility with the remaining digital control circuitry. This technique has the advantage of always using the full dynamic range of the D/A employed. With this system adjustment of the program's gain, both the required signal and the encoding noise will be affected.

The choice of system depends on the code used, in a 14-bit system the analogue technique would be preferable, but if the code used contained 16-bits sufficient dynamic range would always be available even when digital scaling is employed.

5.1.4 Digital Spectral Shaping

With most program material no additional filtering or spectral shaping of the input signal is required. However, some recording processes introduce spectral biasing of the low or high frequency components of the input signal. In addition the user may wish to change the shape of the signal spectrum, to correct for limitations in speaker systems or as personal preference. To cater for this need most audio systems provide variable filters to shape the input signals frequency spectrum. These filters often take the form of variable slope low and high pass filters, more advanced systems also provide mid-frequency adjustment and tilt control. It is often required to use more than one of these filters simultaneously, so analogue systems provide a cascade of different filters which are first, or more commonly second order sections, giving a maximum slope of 6 dB or 12 dB per octave.

The transfer function of a typical analogue filter which can produce the required response consists of two quadratic functions, having two poles and two zeros. It is conveniently expressed in terms of the Laplace transform as:-

$$H(S) = \frac{a_2S^2 + a_1S + a_0}{b_2S^2 + b_2S + b_0} \qquad 5.1$$

The corresponding digital filter can be derived in terms of the z-transform to give the general form of the new transfer function as:-

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{B_0 + B_1 z^{-1} + B_2 z^{-2}} \qquad 5.2$$

In such a filter the coefficients A_0 and B_0 control the overall gain of the filter and are chosen with A_1, B_1, A_2 and B_2 to produce the required frequency response. A wealth of literature on filter design can be used to determine the position of the poles and zeros necessary to give the required frequency response. (Ref. 5.1).

Prior to translating the transform function into a realizable digital circuit it is important to consider the type of errors which can be introduced. There are three main types of this error:-

1. Quantization of the coefficients, this is analogous to a component in an analogue filter which does not have exactly the required value. This will alter the pole and zero positions and thereby change the filters response.

2. Quantization of the products and sums within the filter. This round off error is introduced by the arithmetic used within the filter. If two's complement arithmetic is used, partial sums can result in overflow as long as the final result remains within the permitted number range. Overflow does not occur in multiplication since the output word is re-scaled, but this need to round off the numbers introduces errors. The effect of these errors is accumulative resulting in additional noise appearing at the filter's output.

3. Oscillations within the filter, known as limit cycles can occur when the input to the filter is small. The finite quantization

within the filter and its feedback structure can result in an oscillation which is sustained when the input signal is removed.

Optimization techniques (Ref. 5.2) can be used to reduce the effects of 1. to an acceptable level. The effects of 2 depend on the arithmetic used within the filter and the number of additional bits provided for intermediate results, this also affects the production of limit cycles. In addition there are many filter structures which give the required transfer function. Many studies have been made to determine the most efficient filter structure (Refs. 5.3, 5.4, 5.5).

One such filter, derived by the transpose system (Ref. 5.4) is particularly attractive and is briefly considered. This type of filter is conveniently implemented in its canonic form and is shown in Figure 5.1. The processing which is required to implement this filter is:- five multiplications, three additions and two delays. To meet the high speed processing requirements of such filters specialised L.S.I. circuits have been developed (Refs. 5.6, 5.7) which contain all the required hardware for filtering. These circuits only need to be provided with the input data and coefficient values. The complete range of filter functions could be produced using this system, the coefficients of each filter would be stored in a "library" of coefficients held in a data store.

Another possible way of implementing the digital filters is to use high speed bit slice processors. This would result in a more flexible system.

5.1.5 The Mixing of Digital Signals

Two, or more digital signals can be mixed by adding each individual input sample together to produce a single output word. Scaling each input word prior to addition enables controlled fades between individual input signals. The provision of the adders would, again,

need a high speed A.L.U.

SUMMARY

It has now been demonstrated that all the functions found in an analogue system can be replaced by digital circuitry. There are a number of advantages in using a digital system. In analogue circuitry, great care has to be taken to realise the required characteristics while maintaining the required signal quality. As a result the circuitry is costly and difficult to mass produce.

The circuit construction requires careful layout which determines the location of the user controls. This is not true of a digital system, once a flexible processing unit has been developed, it can be mass-produced. The required functions are under software control and consequently they can be adapted for specific needs, specialised filter structures can be developed, such as linear phase filters using transversal filters, considered necessary by some experiements, further the user is free to develop his own software, which could store individually tailored responses.

5.2.1 Digital Power Amplifiers

To complete the generation of audio, all the systems proposed so far require the digital signals to be converted into low-level analogue signals. These signals need further processing by an analogue power amplifier to produce sufficient power to drive a loudspeaker. These power amplifiers require careful design to ensure they do not limit the system's performance. This necessitates them being complex and costly.

An alternative approach is possible by using a power switch, controlled by the output of a noise shaping encoder, to supply pulses directly to the loudspeaker. Consider the transfer function of a noise shaping encoder,

$$Y(z) = X(z) + H_{NS}(z) \cdot Q(z) \qquad 5.3$$

The output (Y(z)) of the encoder contains the required signal information and additional out-of-band encoding noise. This additional noise is normally removed by filtering the output data, resulting in the required, output signal. If the unfiltered signal is applied to a system which only has a low-frequency response the need for additional low-pass filtering is eliminated; such a system is a conventional loudspeaker. The frequency response of a loudspeaker is limited by the mass of its cone to the audio spectrum. Thus the effect of applying the one bit output of a noise shaping encoder to a loudspeaker will be the reproduction of signals contained in the message band and the removal of the unwanted out of band noise. To transfer sufficient power into the loudspeaker the voltage levels of the one-bit code needs to be increased. This can be done by using the output of the noise shaping encoder to control a switch which applies a large negative or positive voltage to the loudspeaker. This type of output circuit has previously been used with little success in conjunction with pulse width modulation. It is useful to review the limitation of pulse width modulation.

5.2.2 Pulse Width Modulation

A pulse-width system encodes an analogue signal into a series of pulses whosewidth is proportional to the amplitude of the input signal. Initially the input signal is set to +V and the modulator re-set, this indicates the start of a new pulse. This pulse is integrated and compared with the level of input signal. When the two values are identical the pulse is curtailed. The position of the rising pulse edge is determined by the clocking frequency and the falling edge by the signal's amplitude. Pulse width modulation is a form of Asynchronous delta modulation (Ref. 5.8), asynchronous because the falling edge of the output pulse occurs without reference to the system clock. A simple pulse width system is shown in Figure 5.2. The output stage simply switches the speaker between the two supply rails at a rate determined by the comparator's output. Unfortunately

pulse-width systems generate a large spectrum of cross modulation products including terms such as $f_m \pm f_s$, $f_m \pm 2f_s$ . . . , etc. (where f_s = signal frequency) (Ref. 5,9). The higher order terms are of low-amplitude and the relative amplitudes of all these products changes with the modulation index used. Only the in-band modulation products are important as these will result in additional noise at the system's output. Some of these products are not harmonically related to the signal frequency so they are subjectively less acceptable than equivalent amounts of harmonic distortion. To reduce these products to an acceptable level the modulation index must be kept small; this means that the modulator frequency must be much greater than the maximum input frequency used, consequently the power available from a given supply to the loudspeaker will be reduced. One of the main drawbacks to pulse width systems has been in the development of a suitable high speed switch, conventional transistors have severe frequency limitations.

5.2.3 V-MOS Power Fets

The development of the V-MOS transistor has made high-power switching circuits practical. It is informative to investigate their structure before describing their operation and limitations.

Siliconix introduced the first V-MOS power devices in 1976. Originally only n-channel devices were available, however, recent developments in semiconductor technology have resulted in the production of the complementary p-channel device. The V-MOS transistor is a development of the normal MOS power transistor. Instead of producing the transistor with a lateral structure, whose precision depends on masking techniques, a vertical (VMOS) structure is employed, this is shown in Figure 5,3. This structure allows the device to be produced smaller and with greater precision by using diffusion techniques. Consequently the channel length is that of the extremely thin body of the transistor. This results in a low on-resistance, and a small gate capacitance because of the

reduced size and reduced overlap between the layers. Besides this VMOS transistors are more tolerant of overload since the ON resistance has a negative temperature coefficient. This means the drain current becomes less as the device temperature increases, so making the transistor self-protecting. The summary in Table 5.1 compares the main parameters of bipolar and VMOS transistors.

P-channel VMOS transistors are similar in construction to their n-channel equivalents except that their n and p regions are interchanged. In p-channel devices the ON resistance, for a given channel area, is twice that of the equivalent n-channel device. The reason for this is that in the n-channel device the majority carriers are electrons, but in the p-channel device the majority carriers are holes which have a lower mobility. Manufacturers eliminate this difference in on-resistance by increasing the channel area of the p-channel device, however, this increases the gate capacitance and therefore makes driving the device more complex.

For switching speeds up to 30 MHz the equivalent circuit of the VMOS device is a single capacitor at the gate input controlling an ideal switch with a series resistor equal to the on-resistance. At higher frequencies the inductance of the package becomes significant.

5.2.4 Output Circuits

The circuit of a typical switching output stage is shown in Figure 5.4. The two switches are closed alternatively at a high frequency, to produce in R_L a waveform whose duty cycle is averaged out (by the acoustic response of the load) to give the required low frequency signal. The drive waveform for the switches has only two states and is derived from the output of the code converter used. This signal could be obtained from a d.s.m. second order system or a pulse-width modulator.

The efficiency of this type of circuit is high and can be calculated by assuming the output voltage is slightly reduced due to the

switches on resistance. The theoretical efficiency in this case (η) is given in equation 5.4:-

$$\eta = \frac{R_L}{R_L + R_{ON}} \qquad 5.4$$

for a load impedance of 15Ω the efficiency becomes 88%. This assumes ideal switching edges but in practice the finite rise and fall times of the switches means that both devices will be switched on together for a short time in each transition.

The output switches in Figure 5.4 could be constructed out of two n-channel devices, as shown in Figure 5.5a or a complementary arrangement using both p and n-channel devices illustrated in Figure 5.5b, each circuit having its advantages. When two n-channel devices are used it is possible to match their performance accurately since the input capacitance and on-resistance are the same. This advantage is at the expense of a more complex drive circuit which must provide complementary switching pulses to switch each device separately. Unfortunately the voltage swing of the one drive signal must be greater than the other to ensure correct operation. The drive circuitry in a complementary arrangement can be common to both transistors, the two gate connections being connected together; however, the output signal is not symmetrical since the n-channel device is switched on and off more easily. The different methods of driving VMOS transistors are considered in the next section.

5.2.5 Drive Circuits

To preserve the fast switching characteristics of VMOS devices the gate drive waveforms must have comparably fast transition times. This is a major problem since the gate capacitances are large (≈65 pf). In effect the shape of the output pulse will be solely dependent on the drive waveform. As the input impedance at high frequencies of the devices is low the drive circuit needs to be able to inject a high current whilst switching the device on, then maintain a small current to replace any leakage and finally provide a low

resistance to remove the stored charge in the gate as quickly as possible. The simplest method of driving the VMOS transistor consists of an open collector T.T.L. gate with a pull-up resistor. This is shown in Figure 5.6. To ensure a fast turn on time the resistance of the pull up resistor must be low to maintain a high current drive. This results in the resistor dissipating excessive power when the driver transistor is on. The turn off time is determined by the on resistance of the driver transistor. An increase in drive current can be obtained by using a totem pole arrangement employing an additional high speed transistor. This circuit can be improved by boot-strapping the supply to the totem pole stage thus providing a higher voltage to the gate of the VMOS transistor. This is possible because the pulse required is of short duration. A low on resistance in the drive transistor can be assured by paralleling several open collector gates together. The arrangement is shown in Figure 5.7.

The complementary drive pulses required by the n-channel system can be obtained by using two identical drive stages, supplied with complementary signals derived by inverting one of the data inputs, or using a third VMOS transistor as a phase inverter. The latter arrangement is shown in Figure 5.8, the drive to both the gates would then be supplied by the circuit in Figure 5.7.

Since it is possible to obtain small signal low power VMOS transistors which have lower input capacities, they can be used to drive the power versions when driven by the same arrangements discussed above, this may permit increased switching times. The results obtained with these circuits are described in Section 5.4, where an optimal arrangement is constructed and tested.

5.2.6 Output Filtering

It is necessary to provide some filtering at the output of the power switch before the loudspeaker is connected. This is required to

reduce the amplitude of the fundamental switching frequency applied to the load, to prevent radiating interference. The filter need only consist of a parallel tuned circuit in the output circuit offering a high impedance at the high frequency switching transients. A suitable arrangement is shown in Figure 5.9. More sophisticated filters are undesirable since the additional capacitance they would present to the output switch would adversely affect the edges of the output signal. To further reduce the radiated energy all the connections to the loadspeaker can be made with screened cable.

5.3.1 Practical Digital Power Amplifiers

The previous sections have shown that a digital power switch can be constructed using available components. Before these ideas can be transformed into a practical system some additional factors must be considered. Three input signals have been considered; pulse width modulation, delta modulation and higher order systems. Pulse width modulation is not considered practical since it can only perform when used with low modulation indices and in addition an exceptionally high clock frequency is required when encoding 14-bit P.C.M. ($\simeq$ 500 MHz). It is therefore not considered further. Delta modulators can be constructed simply in both analogue or digital form, however, they are unable to produce high quality at realistic clock frequencies ($<$ 8 MHz). They may be used to advantage in the future to provide efficient low-cost amplifiers in telephony systems. The most suitable code for Hi-Fi audio amplifiers is produced by higher order systems, of these a second order system has been shown to perform well at clocking frequencies of 4 MHz. This code is used in the proto-type systems developed in the next section.

5.3.2 Experimental Drive Circuits

All the drive circuits in Section 5.2.5 were constructed and tested. Although they all functioned one arrangement was found to be

more successful, this circuit was used in the final prototypes. To obtain the required fast edged switching pulses very low value pull up resistors were required on the TTL gates, these combined with emitter follower stages and boot strapping provided a pulse with a rise time of 10 nS. The final circuit is shown in Figure 5.10 an example of the switching pulse is given in Figure 5.11. This circuit was then used to drive a pair of low-power complementary VMOS transistors. Connecting the gates of these transistors changed the original switching pulse (shown in Figure 5.11) introducing a change of slope at the lower region of the rising edge, illustrated in Figure 5.12. Investigations into the cause of this change (Ref. 5.10) revealed that the gate capacitance changes with the applied gate voltage.

The gate capacitance has been shown to consist of a combination of two capacitors, the gate source capacitance (C_{gs}) and the gate drain capacitance (C_{gd}). C_{gs} varies little with voltage but C_{gd} is a strong function of voltage. As the gate voltage is increased from zero current is transferred to the gate capacitance before the device switches on this capacitance is dominated by C_{gs}. However, when the threshold voltage is approached, C_{gd} increases, as this extra capacitance is charged the voltage on the gate remains constant since the driver is already current limiting, once charged the voltage increases to its maximum. The resulting output signal has a slower rise time than the original drive signal. This problem is not easily resolved, improvements are only possible by increasing the amount of current available to the gate during switching. It was, therefore, decided to drive the output transistors directly with the open collector circuit eliminating any intermediate driver VMOS stages.

When a single VMOS stage was used as a phase inverter driving two n-channel VMOS transistors (Figure 5.8) similar problems were encountered.

The more successful arrangement of using two identical T.T.L. driver stages working in antiphase was adopted. The limiting factor in the fast switching of VMOS devices is providing sufficient current to charge their gate capacitance.

5.3.3 The Prototype Power Switch

To investigate the performance of a practical system two prototype amplifiers were designed using the drive circuits described in the previous section. The first, shown in Figure 5.13, used two n-channel devices; the second circuit, shown in Figure 5.14, used complementary VMOS transistors.

The calculations in Section 2.2.4 explained why it was important to maintain equal rise and fall times in the output pulses of the code. Since the experiments in the previous section suggested this may not be possible, a differential output circuit was constructed. With reference to Figure 5.15, the loudspeaker is connected between two identical power switches. The voltage appearing across the load is the sum of the individual outputs of both switches. Since the one switch is activated by the incoming data and the second by the inverted data this voltage is always the sum of a rising and falling transition in the output data, thus the effect of any imbalance in these stages is reduced.

Both the complementary and non-complementary output circuits produced identical output pulses. The rise and fall times of these pulses follow the shape of the drive pulses; an example of them is given in Figure 5.16. This confirms that the rise and fall times in the output signal are different.

A series of practical measurements showed that the harmonic distortion from the differential switch was considerably lower than

from the non-differential switch. This improvement in performance can be seen by comparing the results obtained using both types of output circuit which are summarized in the table below.

Measurement	Single Stage	Differential Stage
Peak S/N	-45 dB	-66 dB
Idle Channel Noise	-66 dB	-68 dB
2nd Harmonic	-50 dB	-74 dB
3rd Harmonic	-70 dB	-84 dB

These results show that the second harmonic is reduced by 24 dB when the differential output circuit is used. An example of the harmonic distortion introduced by the switch is given in Figure 5.17.

The ability of the output filter to remove the switching frequency is demonstrated in Figure 5.18. This diagram shows the signal at the input to the filter and the resulting signal at its output. It can be seen that the filter attenuates the fundamental switching frequency and the remaining components are at a reduced level; this avoids driving the load into its non-linear region and reduces the radiated interference.

The noise introduced by the switch when driven by a square wave at half the modulator's clock frequency is minimal. This corresponds to the idle pattern from a 1st order modulator; the level of this noise was measured at -86 dB which is comparable with the results obtained without the power switch. However the idle pattern of the second order system is more complex than a simple square wave and when this was applied to the power switch the idle channel noise increased by 18 dB.

Since this increase in noise was not observed in the output circuits used in Chapter 4, it was attributed to some characteristic of the power switch itself.

A further indication of the level of noise introduced by the power switch can be obtained by considering the variation of S/N ratio with signal level. This is plotted in Figure 5.19. The results are consistently 15 dB below those obtained without the power switch. This suggests that the power switch adds a constant amount of additional noise. The absence of any noise when a high frequency square wave is used to drive the switch indicates that the noise is not inherent in the VMOS transistors, i.e. thermal and shot noise is at an insignificant level. Observations on the shape of the additional noises spectrum (Figure 5.20) indicated it had the same shape as the idle channel noise measured in the modulator's output waveform (Section 2.2.5), but at a higher level. This indicated some amplification of the inherent noise contained in the modulator's output signal.

A possible mechanism for the production of noise by the power switch is as follows:- when the transistor switches from off to on it is biased in a linear mode for a small period of the switching time. Under these conditions any noise applied at the input of the switch will be amplified and appear at the output.

To test this hypothesis, the effective gain of the output switch in its linear mode was reduced by inserting a source resistor in series with each transistor. This had the effect of introducing negative feedback into the output circuit. The value of resistor was chosen to reduce the linear gain of the switch to unity. This had no effect on the level of noise produced at the output, indicating that some other noise mechanism was operative.

Both the complementary and non-complementary output circuits produced a high idle channel noise and since its level dominated the results obtained it was not possible to investigate any differences in their performance.

Although no explanation of the cause of the high noise floor in the output circuit has been found, its performance indicates that a successful all digital system can be produced.

Parameter	Bipolar	VMOS
Input resistance	$10^3 \ldots 10^5$ Ω	$10^9 \ldots 10^{11}$ Ω
Power amplification	100...200	$10^5 \ldots 10^6$
Switch-on time	50...500 ns	4 ns
Switch-off time	500...200 ns	4 ns
ON resistance	0.3 Ω	3 Ω
Breakdown characteristics	bad, second breakdown	good
Parallel operation	only with special circuits	no difficulty

Table 5.1

Comparison of parameters of bipolar and VMOS transistors

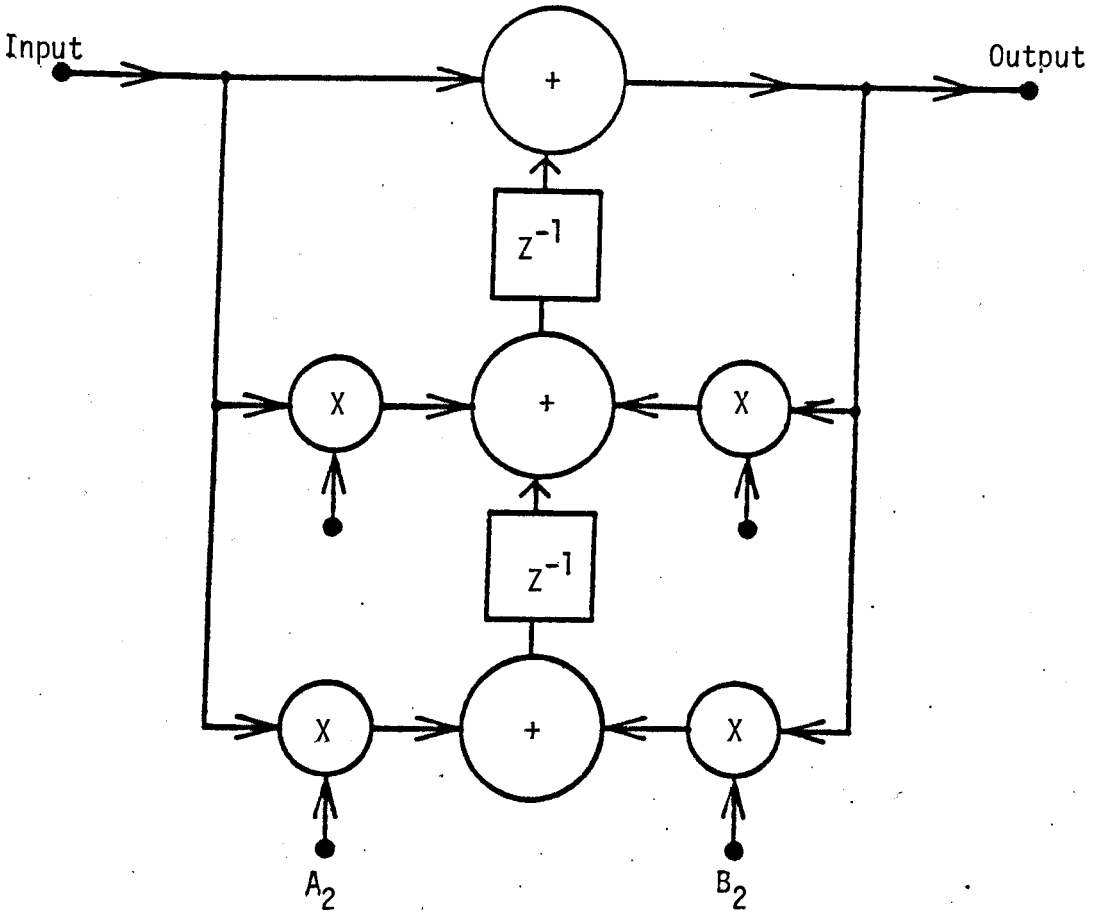


Figure 5.1 A digital tone filter.

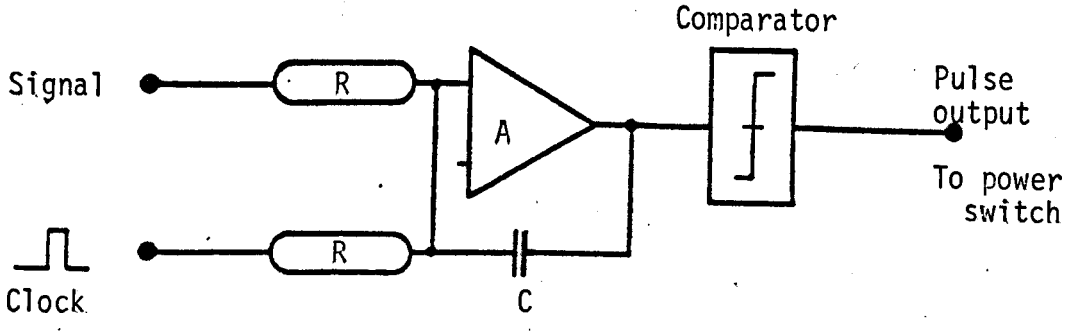


Figure 5.2 Simple pulse width modulator.

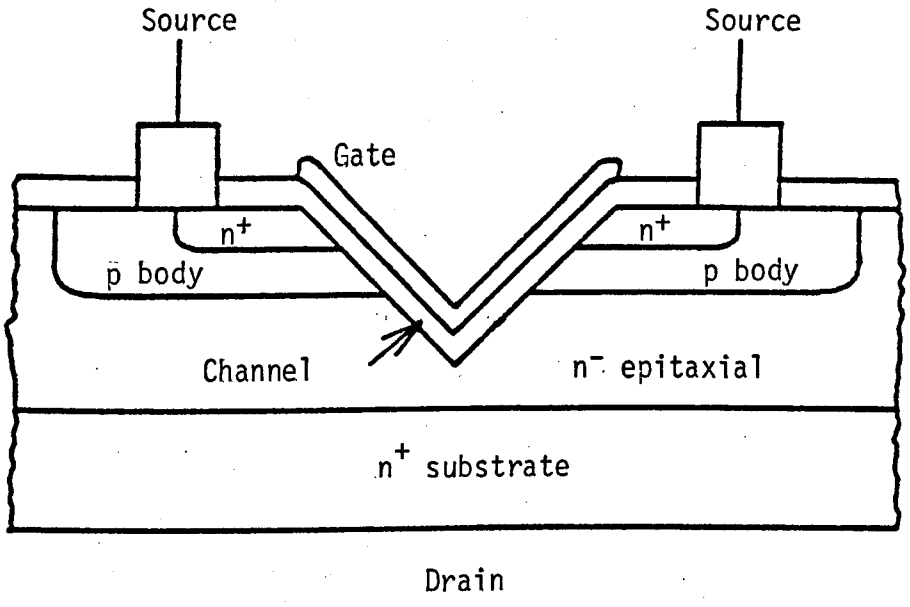


Figure 5.3 Structure of a VMOS transistor.

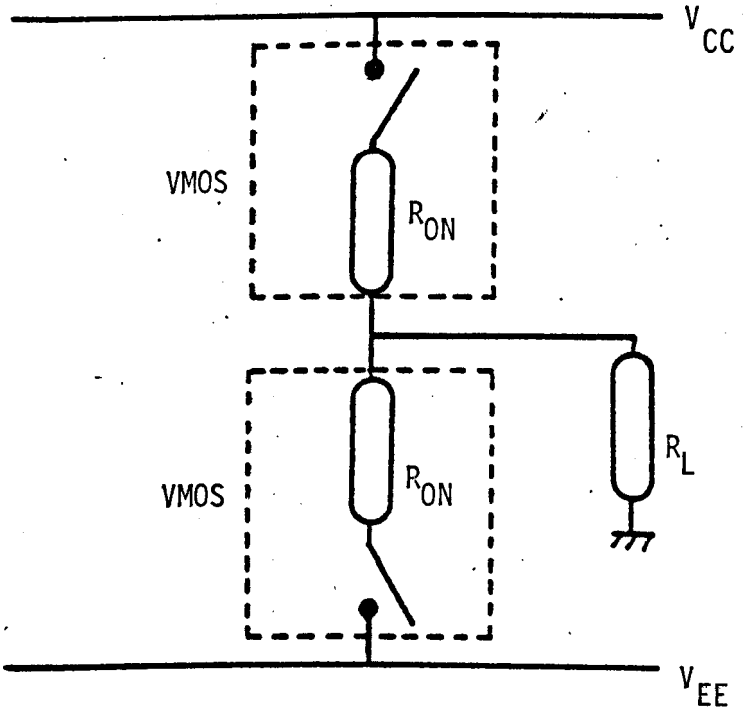


Figure 5.4 Diagram of an ideal power switch.

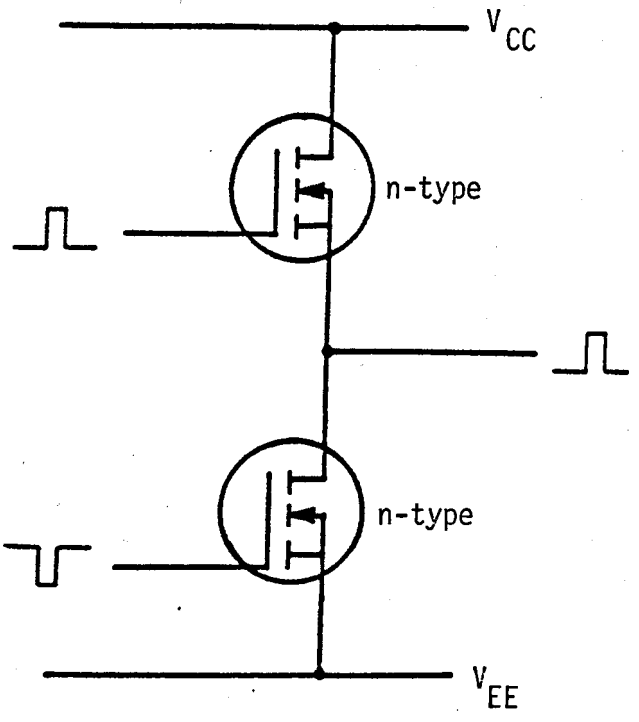


Figure 5.5a Connecting two n-channel devices to form a power switch.

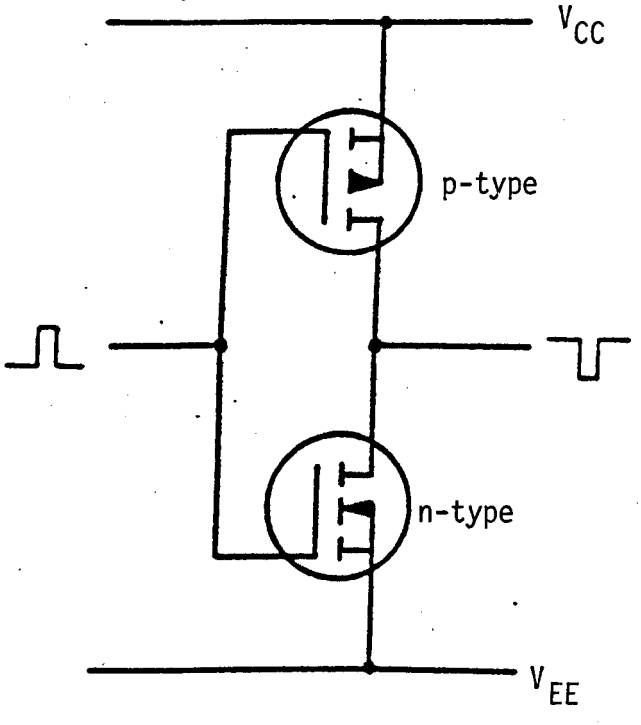


Figure 5.5b Connecting complementary devices to form a power switch.

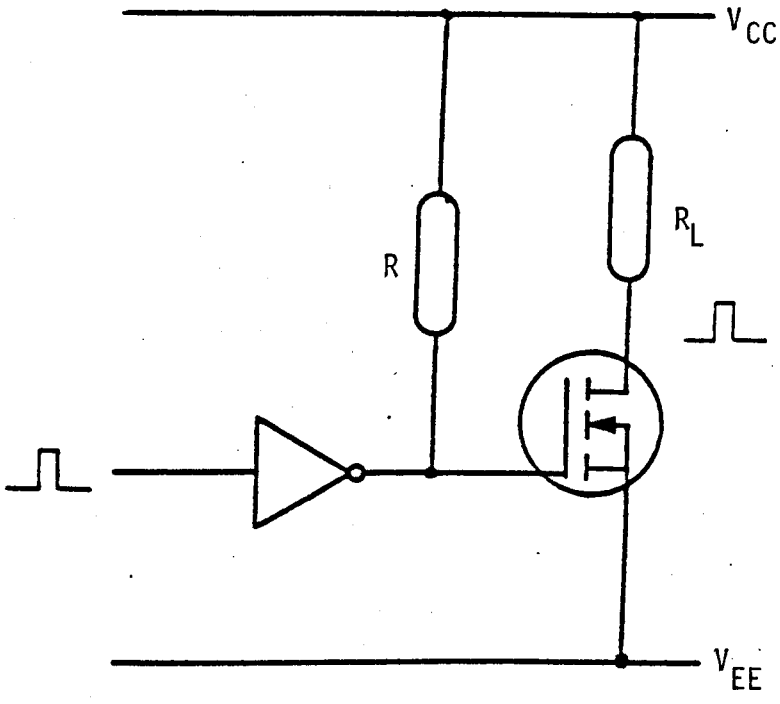


Figure 5.6 Power switch drive circuit using an open open collector gate.

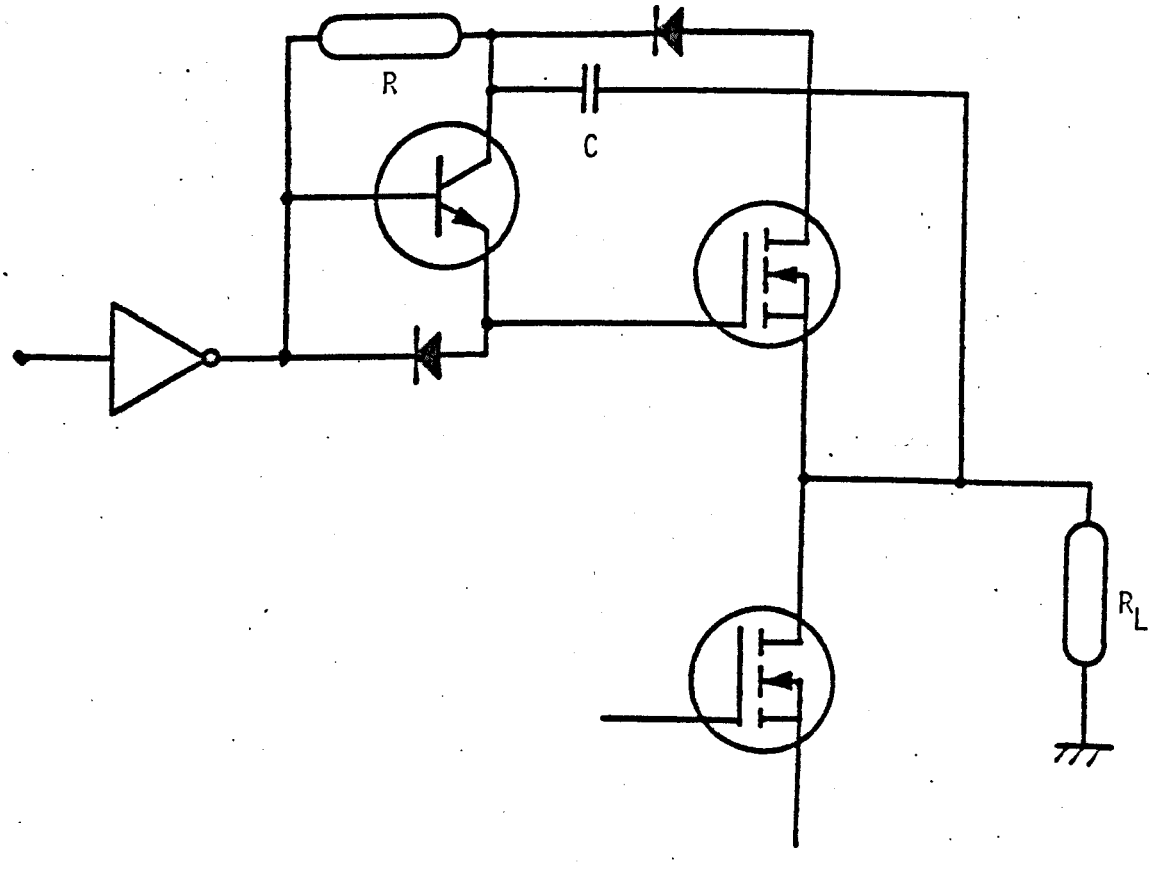


Figure 5.7 Use of active pull-up with bootstrap to improve the rise time of the driver stage.

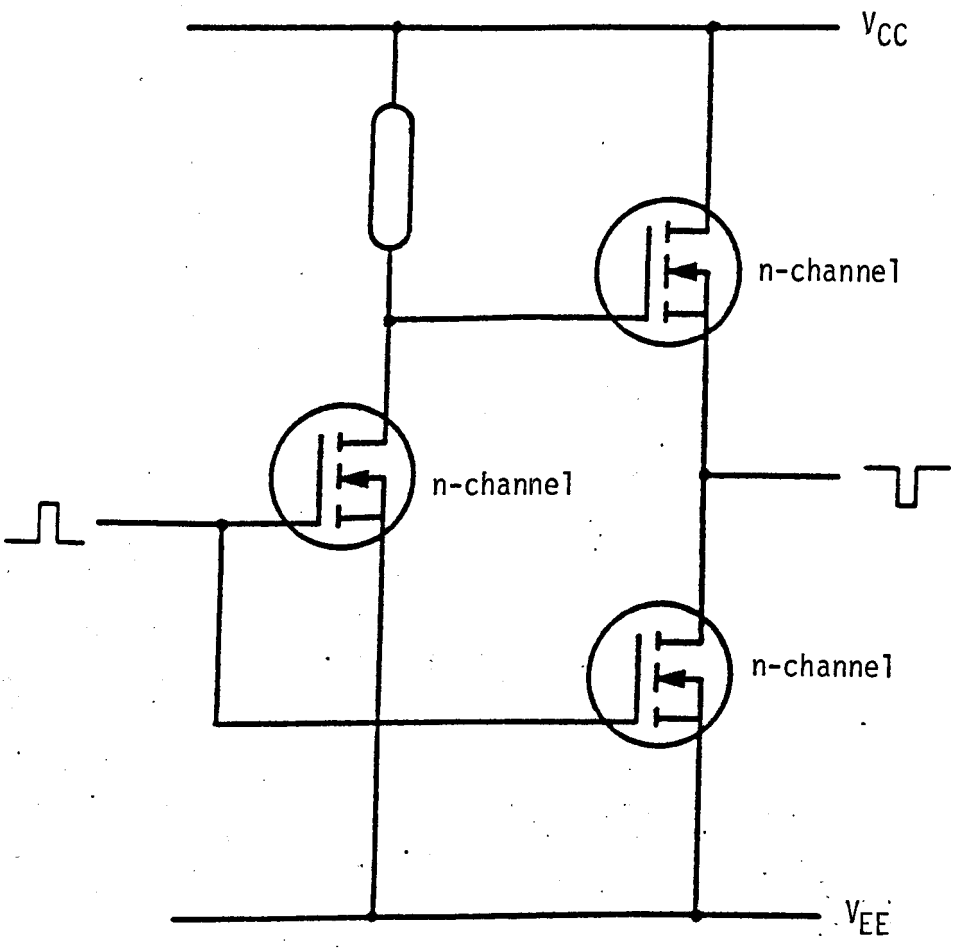


Figure 5.8 Use of a phase inverter to obtain the complementary drive signals required by the power switch.

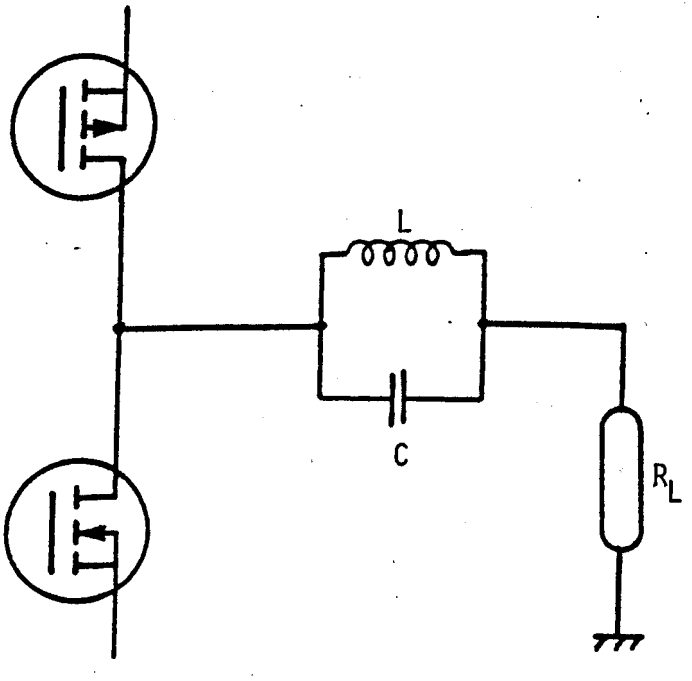


Figure 5.9 Power switch output filter.

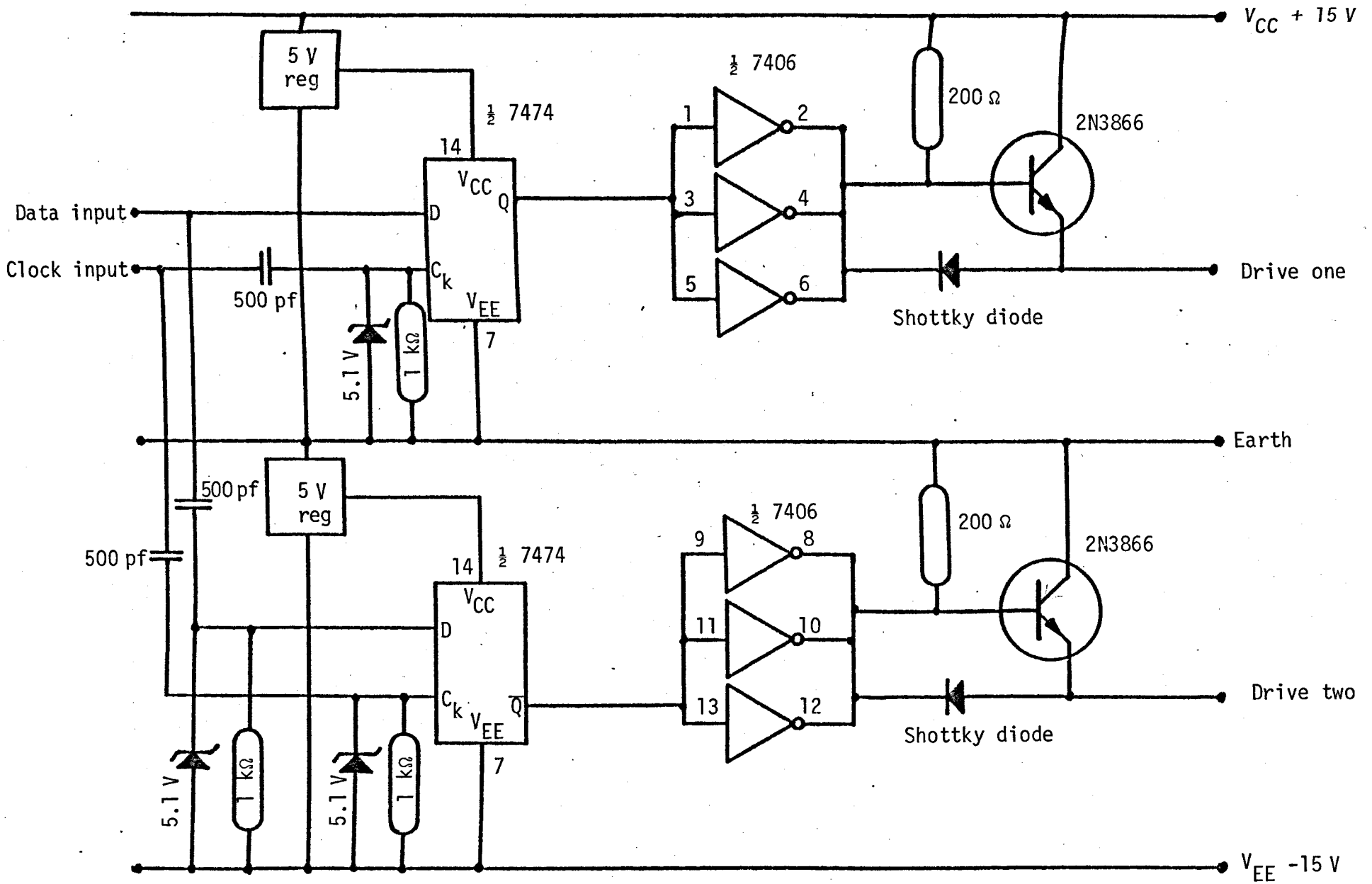


Figure 5.10 Circuit of practical power switch driver.

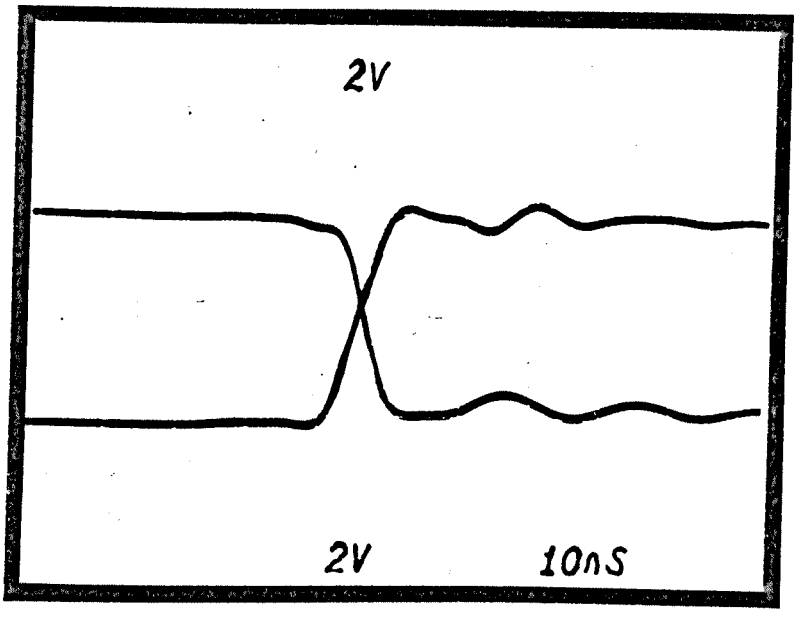


Figure 5.11 Example of power switch drive signal.

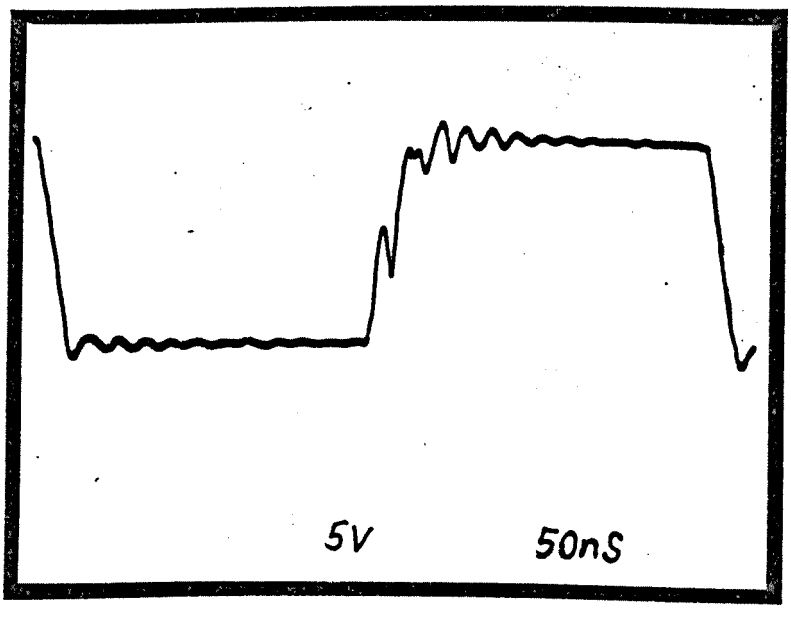


Figure 5.12 Effect of driving a VMOS gate on the shape of the drive signal.

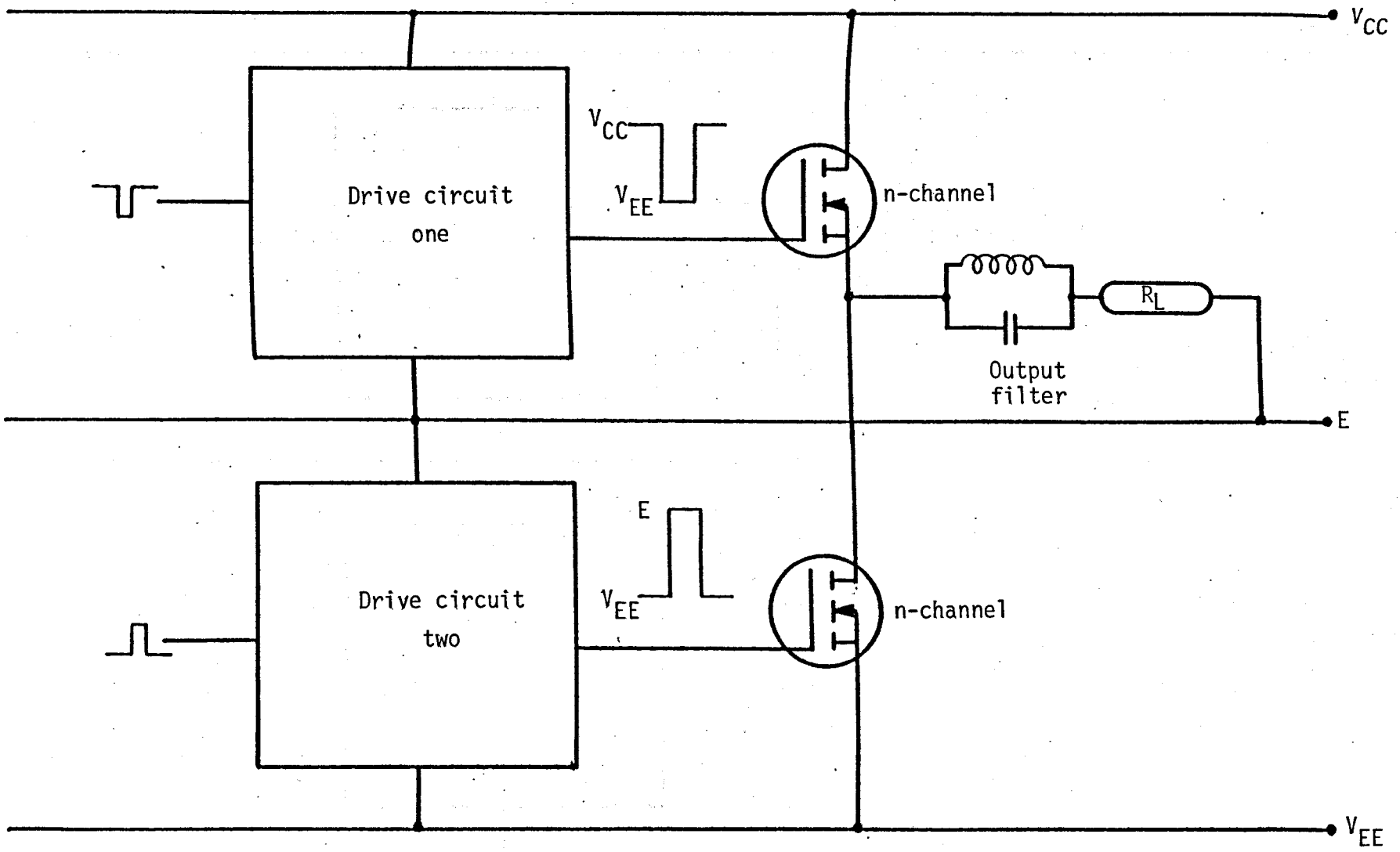


Figure 5.13 A practical n-channel output stage.

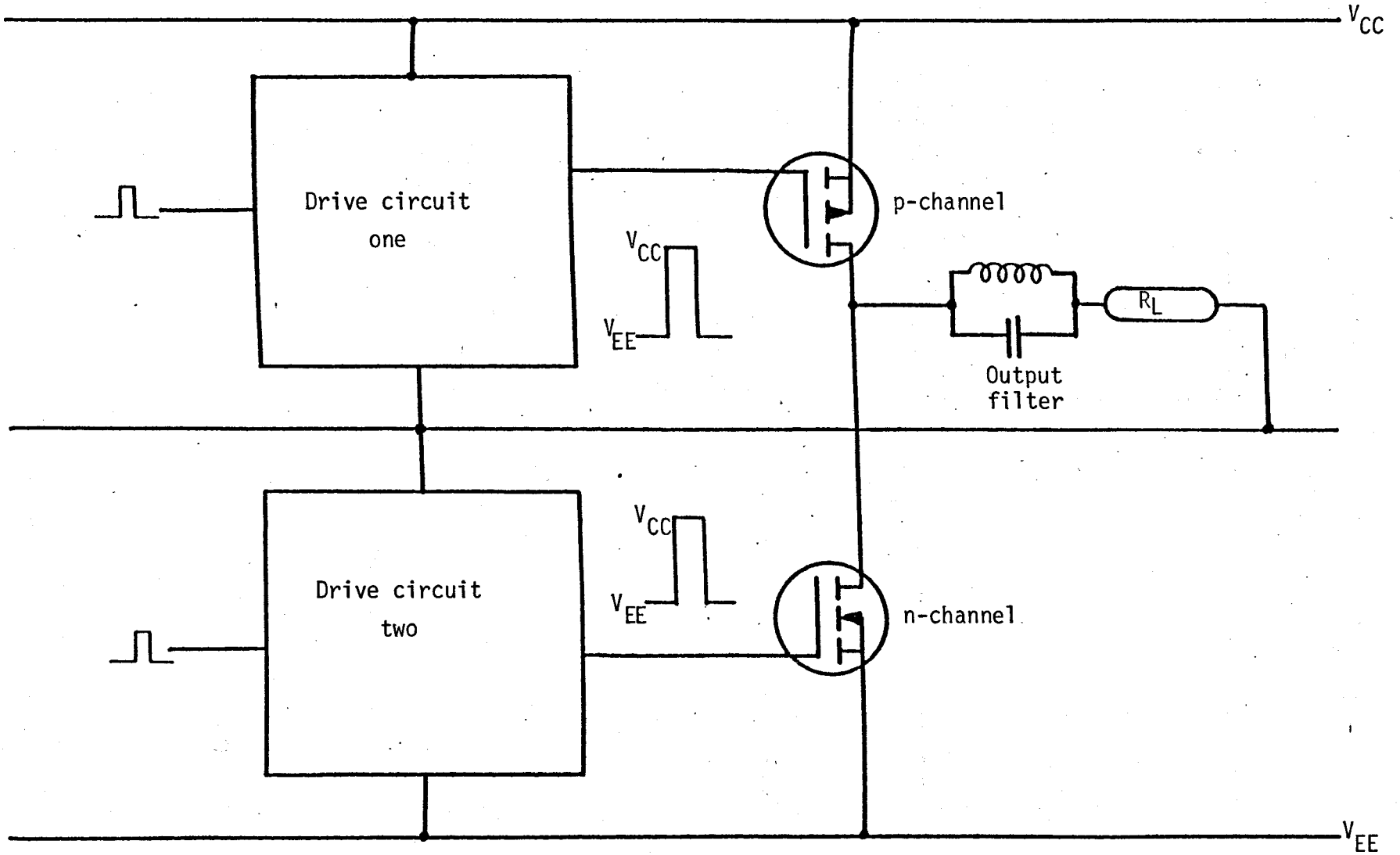


Figure 5.14 A practical complementary output circuit

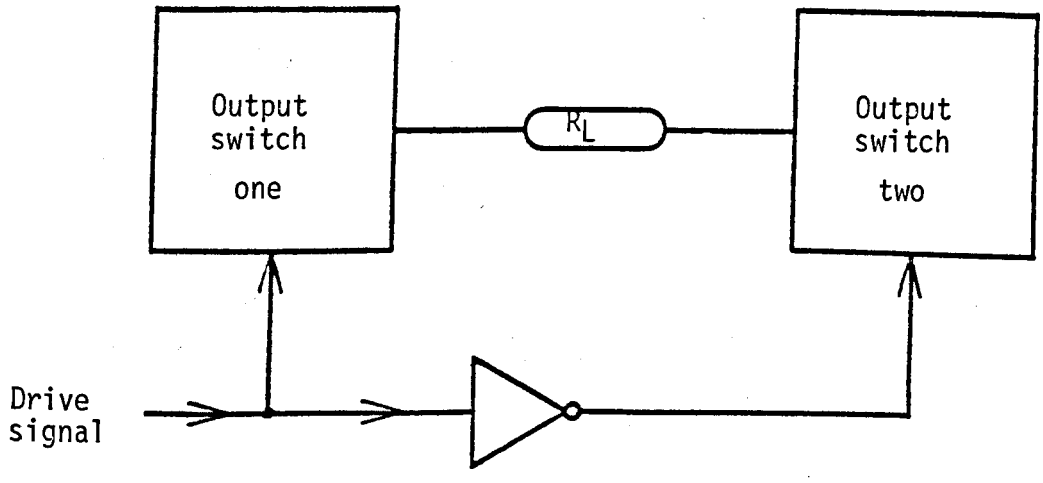


Figure 5.15 Use of a pair of output switches to eliminate the effect of unequal rise and fall times in the output signals.

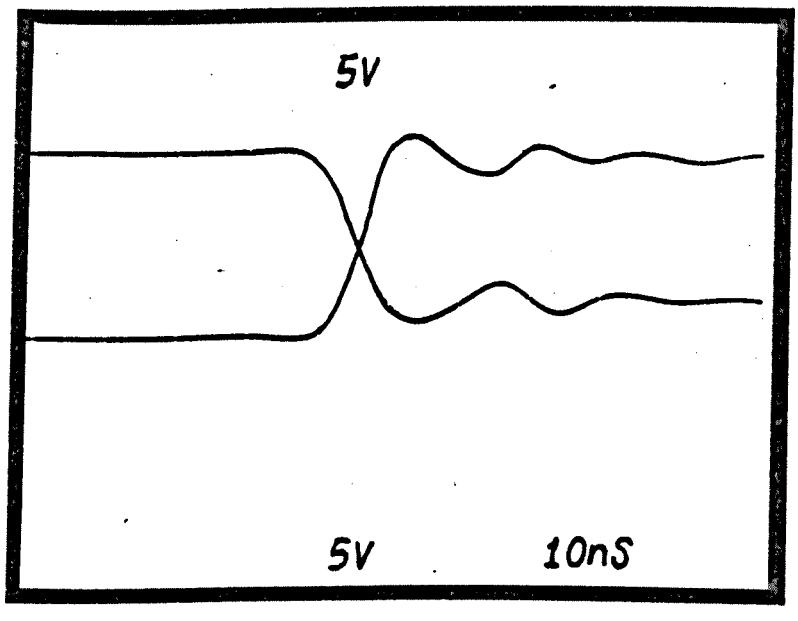


Figure 5.16 The power switch output waveform.

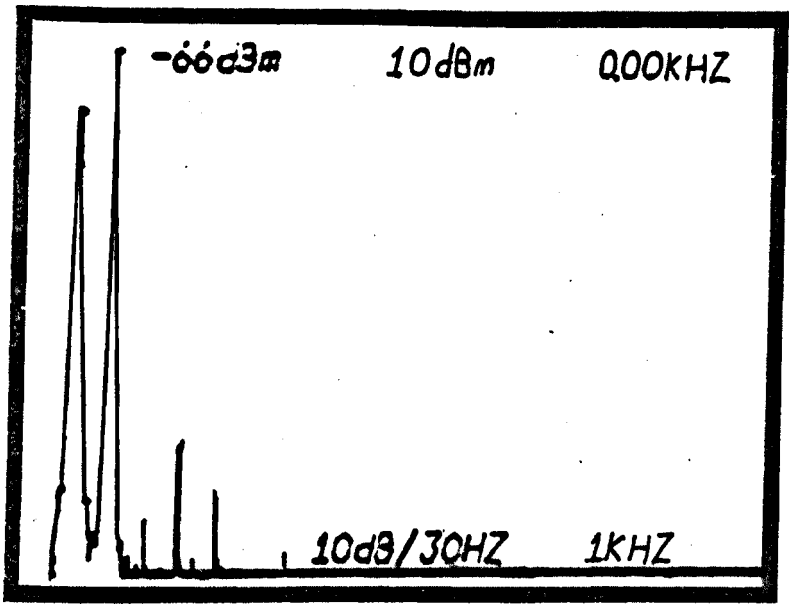


Figure 5.17 Spectrum of the power switch output.

Fundamental level	=	- 2 dB
2nd harmonic	=	-74 dB
3rd harmonic	=	-84 dB
4th harmonic	=	-
5th harmonic	=	-90 dB

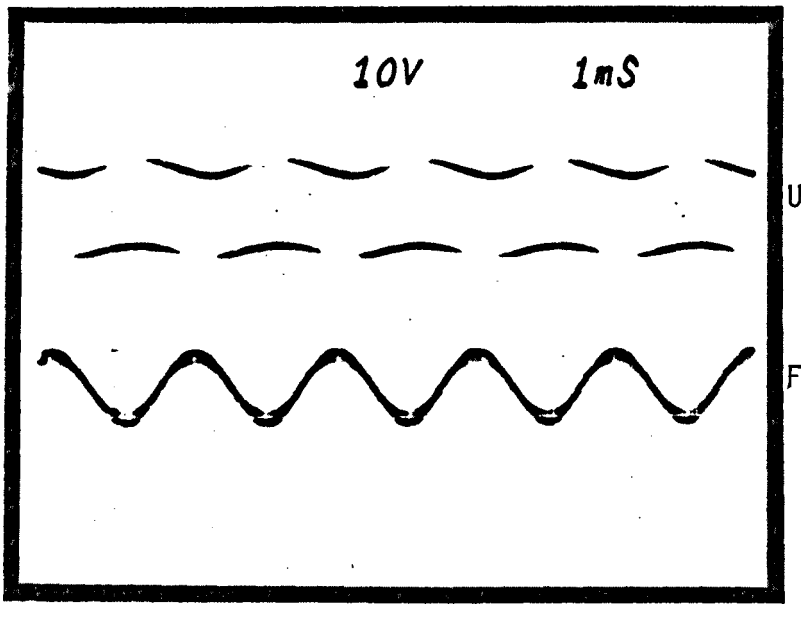


Figure 5.18 The effect of the output filter on D.S.M. output.

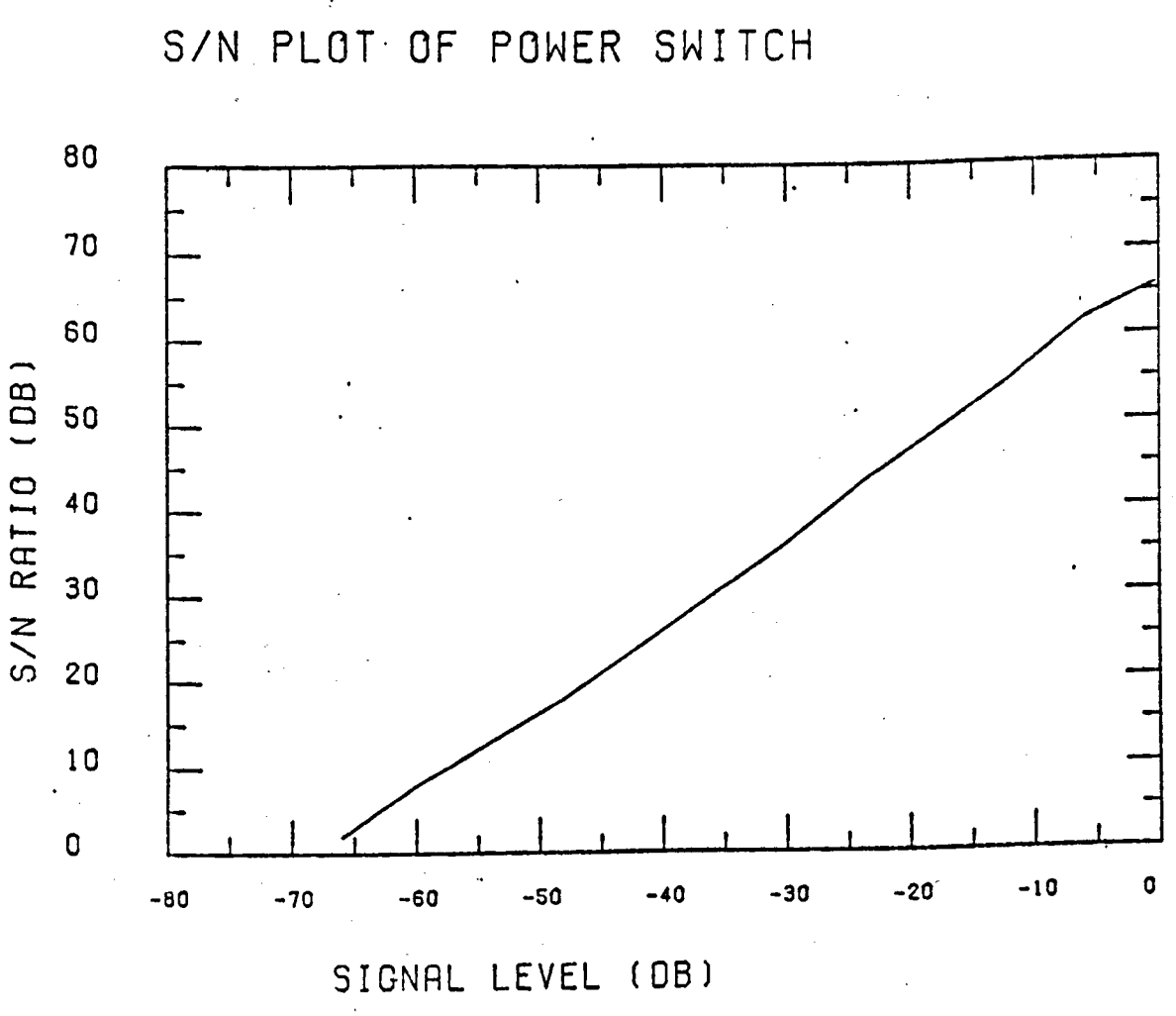


Figure 5.19 S/N of power switch output.

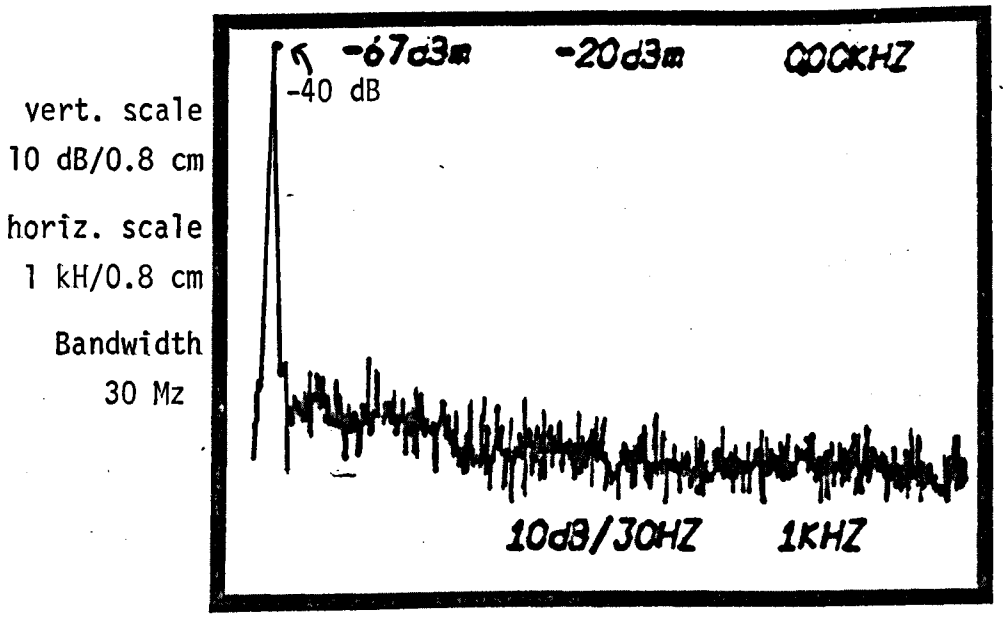


Figure 5.20 Idle channel noise spectrum from power switch.

CHAPTER 6

DISCUSSION AND SUGGESTIONS FOR FUTURE WORK

6.1 Discussion

The saturation of current analogue technology and the subsequent introduction of digital techniques into the domestic Hi-Fi industry have been discussed in Chapter 1. To achieve the maximum penetration of the consumer market the need to develop low cost D/A converters, capable of providing high quality has been suggested. Attention was therefore focussed on the possible use of code conversion techniques to develop an alternative code to P.C.M. which could subsequently be decoded into analogue signals with the minimum of analogue hardware. It is envisaged that such a system would be implemented entirely with digital circuitry, thereby removing the need for any expensive precision analogue circuitry. The code conversion systems considered were chosen to reduce the digital hardware complexity to a level which could be fabricated on a single L.S.I. integrated circuit.

The use of delta-sigma-modulation as a suitable intermediate code was investigated in Chapter 2, where it was confirmed experimentally that a basic d.s.m. was unable to provide the required quality at acceptable clock rates. Methods of enhancing the d.s.m. performance by shifting the low frequency encoding noise out of the message band by applying offsets to the encoder were investigated. These techniques were shown to extend the coder's dynamic range and provide a useful increase in the system's S/N ratio. However, an unfortunate consequence

of using this technique, a sharp dip in the S/N ratio at particular signal levels, was shown to occur whenever the input signal cancelled the applied offset. An optimal offset was chosen and shown to be capable of encoding 13-bit P.C.M. A limitation in the decoding of d.s.m., due to unequal transition edges on the output data was investigated. Theoretical calculations were developed to determine how accurately these edges needed to be matched to preserve the full accuracy of the d.s.m. data. A suitable circuit which cancelled any imbalance in unequal rise and fall times in the d.s.m. output was developed, so eliminating the problem. The results obtained from the circuits described in Chapter 2 highlighted the limitations of the basic d.s.m. and in the improvements which could be obtained using offsets to redistribute any in-band noise. It was concluded that a d.s.m., with suitable offset, could be successfully used with companding systems, where the companding code noise would mask any dip in S/N resulting from using the offset.

Chapter 3 described how the inherent linearity of a d.s.m. over a restricted input range can be exploited to produce an error feed-forward system. The experiments made on a practical system indicated that the modulator's noise spectrum changes according to the level of input signal. This made the error feed-forward technique impractical.

An alternative system based upon the error feed-forward principle was developed to overcome the aforementioned problem. This system, called the residual error encoder, pre-quantized the input signal before applying it to a d.s.m. This restricted the dynamic range of the input signal and enabled the error signal to be easily obtained for encoding by a second d.s.m. The residual error encoder performed well. The encoding accuracy approximated to a 14-bit P.C.M; however,

subjective tests indicated the presence of program modulated noise. This was shown to be caused by low level harmonics being produced by the d.s.m. The level of these harmonics were investigated using a computer simulation of the system and found to be a fundamental limitation in the performance of a d.s.m.

More advanced code converters were considered in Chapter 4. The original d.s.m. used a simple first order filter in the feedback path; a second order noise shaping filter was considered and tested. This system proved that a full 14-bit accuracy encoder was feasible. An increase in low frequency quantization noise at low signal levels, originally observed in d.s.m., also occurred in the second order system. This limited the practical performance below the theoretical predictions but the effectiveness of the noise shaping filter ensured that this increased noise was still below the noise contained in the 14-bit input signal. A new method of stabilizing the second order system was developed which was simpler and more effective than previous methods. The increase in complexity of the second order encoder suggested it required 1600 constituent gates compared to 650 for a first order d.s.m. However this number can still be accommodated on a single L.S.I. circuit.

The possible development of an all digital audio system was considered in Chapter 5. The implementation of all the major components of such a system were discussed and possible problem areas highlighted. A new all digital class D power output stage was introduced; this system eliminates the need to return to the analogue domain for power amplification. The use of this technique is only possible using the single bit code converter described in this report. Although the prototype power switches introduced additional noise, no fundamental limitation in the technique was observed and their development has proved

the feasibility of the technique. Of particular importance to the future development of these power switches is the use of VMOS transistors which operate at the high switching speeds and the use of two switches in anti-phase to reduce their harmonic distortion.

6.2 Future Work

This work has investigated the possibility of new forms of D/A converters. The applications of delta modulation to such converters has been extensively researched and it has been concluded that they have fundamental limitations in performance. Improved code converters using higher order noise filters have been developed. These give more promising results and it has been shown that a second order system can give comparable results with 14-bit P.C.M. Although higher order systems have been considered and appear attractive, since they offer the same performance at lower bit rates, their structures are more complex and are considered uneconomic. These higher order systems have been found to be unstable; however it is anticipated that stable systems could be developed.

Future developments in integrated semiconductor circuits could remove the hardware limitations in higher order systems where their continued development would be practical.

The development of suitable auxiliary hardware in the form of program source selection, volume and tone control has not been considered in detail since it is not fundamental to the main stream of the work. Although the fabrication of such systems is not considered impractical, the investigation into computationally efficient systems is considered new and valuable work.

The continued development of the power switch is considered of prime importance. Such a system offers a new approach to the design of power amplifiers which are efficient and immune to external noise. The mechanism which results in the production of the high idle channel noise observed in Chapter 5 needs isolating and suitable circuits eliminating its effects developing.

In conclusion it is hoped that this work will stimulate the continued development of code-converters for digital audio, leading to the eventual development of an integrated circuit which contains all the digital hardware except the power transistors, to produce an all digital audio system.

REFERENCES

CHAPTER 1

1.1 Dolby, R., "An audio noise reduction system", J. Audio. Eng. Soc., Vol. 15, No. 4, 1967, pp. 383-388.

1.2 Gilchrist, N.H.C., "A/D and D/A conversion for broadcast quality sound", The Radio and Electronic Engineer, Vol. 49, No. 2, Feb. 1979, pp. 77-84.

1.3 SONY, P.C.M. 1600 Data Sheet, 1979.

1.4 Osborne, D.W., "Digital sound signals: further investigations of instantaneous and other rapid companding systems", B.B.C. Research Dept. Report, 1972/31.

1.5 Various authors, "Digital audio technical reports", J. Audio Eng. Soc., Vol. 29, No. 1/2, Jan/Feb 1981, pp. 56-66.

1.6 Stuart, R.D., "Fourier Analysis", Methuen (London, 1961).

1.7 Robinson, D. and Dabson, R., "A re-determination of the equal loudness relations for pure tones", Brit. J. Appl. Phys., Vol. 7, 1956, pp. 166-181.

1.8 Gravereaux, D. et al., "The dynamic range of disc and tape records", J. Audio Eng. Soc., Vol. 18, No. 5, 1970, pp. 530-535.

1.9 Earle, J., "Understanding Hi-Fi specifications", Foundation Press (1978).

1.10 Cattermole, K.W., "Principles of P.C.M.", Iliffe (London, 1969).

1.11 Camenzind, J.R., "Electronic Integrated System Design", Van Nostrand Reinhold Co. (New York, 1972).

1.12 Van de Plassche, R.J. and Coedhard, D., "A monolithic 14-bit D/A converter", IEEE Journal of Solid State Circuits, Vol. SC-14, No. 3, June 1979.

1.13 Gilchrist, N.H.C., "Tests to compare the performance of five companding systems for high quality sound signals", B.B.C. Research Dept. Report EL-143.

1.14 Ely, S.R., "Idle channel noise in P.C.M. sound signal systems", B.B.C. Research Dept. Report EL-135.

1.15 Blesser, B.A., "Digitization of audio, a comprehensive examination of theory, implementation and current practice", J. Audio Eng. Soc., Vol. 26, No. 10, Oct. 1978, pp. 739-771.

1.16 Jayant, N.S., "Adaptive delta modulation with a one-bit memory", Bell Syst. Tech. J., Vol. 49, No. 3, 1970, pp. 321-342.

1.17 Dalton, C.J., "Delta modulation for sound signal distribution. A general survey", B.B.C. Engineering, July 1972.

1.18 Everard, J.D., "Improvements to delta-sigma modulators when used for P.C.M. encoding", Electronics Letters, Vol. 12, No. 15, 22 July 1976, pp. 379-380.

CHAPTER 2

2.1 Everard, J.D., "A single channel P.C.M. codec", IEEE J. of Solid State Circuits", Vol. SC-14, No. 1, Feb. 1979.

2.2 Candy, J.C. et al., "Using triangulary weighted interpolation to get 13-bit P.C.M. from a sigma-delta modulator", IEEE Trans. on Communications, Vol. COM24, Nov. 1976, pp. 1268-1275.

2.3 Everard, J.D., "Improvements to delta-sigma modulators when used for P.C.M. encoding", Electronics Letters, Vol. 12, No. 15, 1976.

2.4 Inose, H. and Yasuda, Y., "A unity bit coding method by negative feedback", Proc. IEEE, Nov. 1963, pp. 1524-1535.

2.5 TEXAS, "The T.T.L. Data Book" (1980).

2.6 Various authors, "Pulse-code modulation for high quality sound distribution: quantizing distortion at very low signal levels", B.B.C. Research Dept. Report 1970/18.

CHAPTER 3

3.1 Black, H.S., U.S. Patent 1686792.

3.2 Seidel, H., "A feed-forward experiment applied to an L-4 carrier system amplifier", IEEE Trans. Communication Technology, Vol. COM-19, June 1971, pp. 320-325.

3.3 Seidel, H., "A microwave feed-forward experiment", Bell Syst. Tech. J., November 1971, pp. 2879-2916.

3.4 Goodman, D.J., "The application of delta modulation to A/D - P.C.M. encoding", Bell Syst. Tech. J., Vol. 48, February 1969, pp. 321-343.

3.5 Van de Plassche, R.J., "A sigma-delta modulator as an A/D converter", IEE Trans. on Circuits and Systems, July 1978, Vol. CAS-25, No. 7.

3.6 Belcher, R.A. et al., "Digital sound: an investigation of delta-modulation/pulse-code-modulation analogue to digital conversion", B.B.C. Research Dept. Report 1980/3.

3.7 Bogner, R.E. and Constantinides, A.G., "Introduction to Digital Filtering", Wiley (London, 1975).

CHAPTER 4

4.1 Tewksbury, S.K. and Hallock, R.W., "Oversampled linear predictive and noise shaping coders of order N 1", IEEE Trans. on Circuits and Systems, Vol. CAS-25, No. 7, July 1978.

4.2 Cattermole, K.W., "Principles of P.C.M.", Iliffe (London, 1969).

4.3 Petit, J.P. and Maitre, X., "Applications of digital filtering and interpolative noise shaping techniques to P.C.M. coding, decoding and filtering", in "Electronics to Microelectronics", Eds. Kaiser, W.A. and Proebster, W.E., North Holland Publishing Company (1980).

CHAPTER 5

5.1 Zverev, A.I., "Handbook of Filter Synthesis", Wiley (London, 1967).

5.2 McClellan, J., "A computer program for FIR filter design", IEEE Trans. on Audio and Electroacoustics, Vol. AV-21, No. 6, pp. 506-526.

5.3 McNally, G.W., "A computer-based mixing and filtering system for digital sound signals", B.B.C. Research Dept. Report 1979/4.

5.4 McNally, G.W., "Digital audio recursive digital filtering for high quality audio signals", B.B.C. Research Dept. Report 1981/10.

5.5 Hirata, Y., "Digitalization of conventional analogue filters for recording use", J. Audio Eng. Soc., Vol. 29, No. 5, May 1981, pp. 333-337.

5.6 PYE (TMC), "TMC 53A, PMOS dual second order digital filter", Data Sheet, PYE TMC Limited.

5.7 Lav, S.Y., "Semi-custom linear and digital I.C. arrays", WESCON Professional Program, San Francisco, California, September 1979.

5.8 Mullick, S.K., "Noise study of an asynchronous delta-sigma modulator", IEEE Trans. on Communications, Vol. COM-28, No. 3, March, 1980.

5.9 Stremler, F.G., "Introduction to Communication Systems", Addison-Wesley (Massachusetts, 1977).

5.10 Severns, R., "Using the power MOSFET as a switch", Electronic Product Design, May 1981, pp. 49-53.

APPENDIX 1

A Review of Delta-Modulation

This Appendix describes the history, important terminology, characteristics and limitations of linear delta-modulation systems.

Delta modulation (D.M.) is a one-bit differential P.C.M. code. Unlike a pulse code modulation system, which uses an n-bit digital code to represent the absolute magnitude of each sample, a delta modulation system only uses a one-bit code to represent each input sample. This single bit indicates in which direction the signal amplitude has changed since the previous sample. Thus the d.m. code contains information about the derivative of the input signal. Consequently the decoder integrates the d.m. output code, to obtain an approximation of the original input signal.

Delta-sigma modulation (D.S.M.) eliminates the need for an integrator at the decoder by integrating the input signal before it is encoded by the d.m. Thus the d.s.m.'s code contains information about the amplitude of the input signal, so as the input signal increases in amplitude the output pulses occur more frequently.

Delta modulation was originally proposed in France at I.T.T. and resulted in two patents in 1946 and 1948 (Ref. A1.1, A1.2). In recent years many different forms of delta-modulation have been proposed (Ref. A1.3), most attempting to reduce the transmission bit rate by tailoring the coder's performance to particular signal requirements. Only the simple forms of linear delta modulation are described in this report since these were the only types considered suitable for low-cost D/A conversion.

Section A1.1 deals with the theoretical operation and performance of linear delta-modulation which forms a natural introduction to the delta-sigma modulation system considered in section A1.2.

A1.1 Operation of Delta Modulation

The structure of the basic linear delta modulation is shown in Figure A1.1. The analogue input signal (x) is compared with an approximation signal (y) generated from a feedback loop in the following manner. The sign of the difference between input and approximation signals is used as the approximation signal. In correct operation the approximation signal attempts to track the input signal. In general the difference or error signal (e) can only take one of two levels as defined by the quantizer, the difference between the two levels is known as the step-size. The sampling rate (f_m) is determined by the rate the latch is clocked. When considering the operation of the d.m. it is often convenient to use approximation levels of +V, -V, however, in practice logic levels of +V, 0, are used. A positive signal will produce a +V output, a negative signal a -V output and zero signals produce a pattern of alternate +V, -V, +V, -V, known as the idle channel pattern.

A1.2 Slope Overload

If the input signal rises steeply then the situation can be reached when the output of the d.m. is always +V, indicating the approximation signal is increasing at its maximum rate. Obviously for a set pulse width and height a "maximum rate of increase" for the approximation signal can be defined. This effect is illustrated in Figure A1.2.

The output of the d.m. can be +V or -V so the height of each pulse (α) will be 2V. If the modulator is clocked at f_m, the interval between pulses (τ_p) is given by:-

$$\tau_p = \frac{1}{f_m} \qquad \text{A1.1}$$

For overloading to be avoided, the rate at which the signal changes, over the time it is sampled for, must be less than or equal to the pulse height. If the input signal has the form:-

$$x_t = A \sin w_s t \qquad \text{A1.2}$$

then the overload point is given by:-

$$\frac{dx_t}{d_t} \cdot \tau_m \leq \sigma \quad \text{where } \sigma_m = \frac{1}{f_m} \qquad \text{A1.3}$$

substituting for x_t and evaluating, A1.3 becomes:-

$$A \text{ Cos } w_s t \cdot \tau_m \leq \sigma \qquad \text{A1.4}$$

In the limit ($t \to 0$) this becomes:-

$$A\, w_s\, \tau_m \leq \sigma \qquad \text{A1.5}$$

The point of overload then becomes:-

$$A_{max} = \frac{\sigma}{w_s\, \tau_m}$$

$$A_{max} = \frac{\sigma f_m}{2\pi f_s} \qquad f_s = \text{signal frequency} \qquad \text{A1.6}$$

The overload point is dependent on the input frequency.

A1.3 Encoding Threshold

Just as there is a maximum signal which can be encoded by a d.m. a minimum signal exists. In order to disturb the idle pattern the input signal must have an amplitude greater than $\sigma/2$. The minimum signal which can be encoded is then given by:-

$$A_{min} = \frac{\sigma}{2} \qquad \text{A1.7}$$

A1.4 Dynamic Range

The ratio of A_{max} to A_{min} gives the range of input signals which can be encoded successfully by the d,m. Using equations A1.6 and A1.7 the coder's dynamic range (D) is defined by:-

$$D = \frac{f_m}{\pi f_s} \qquad \text{A1.8}$$

A1.5 Signal to Noise Ratio

The signal to noise ratio (S/N) obtained will depend on the amount of noise produced by the coder. This additional noise is known as quantization noise. In d,m, the quantization noise has a random amplitude which is dependent on signal level. This can be explained by considering the operation of the modulator at three different signal levels. At zero input signal, the output of the modulator is a square wave at half the sample frequency, in an ideal system this introduces no noise. At high signal levels which cause overload, the noise introduced will depend on the signal's amplitude. At signal levels between these two points the noise introduced will be random and arises from the voltage and time quantization used within the coder. Several contributions have been made towards the analysis of the quantization noise produced by d,m,'s (Refs. A1,3, A1,4, A1.5 for example) the most common method considers a sine-wave input near overload. The widely accepted expression for S/N is:-

$$S/N = \frac{1}{8\pi^2 K_q} \cdot \frac{f_m^3}{f_c f_s^2} \qquad \text{A1.9}$$

f_c = maximum input frequency

K_q = constant

Different experiments arriveat different values for K_q, all approximate to $\frac{1}{3}$.

A1.5.1 Delta-Sigma Modulation

It has been shown that d.m. has the disadvantage of the dynamic range and S/N being inversely proportional to the signal frequency. To effect a solution to this problem a system known as Delta-sigma modulation (d.s.m.) was proposed in 1961 (Ref. A1.6). The linear d.s.m. can be considered as a d.m. preceded by an integrator, a suitable arrangement is shown in Figure A1.3. With this new arrangement the approximation signal attempts to track the integral of the input signal. The decoding of the output of a d.s.m. therefore requires the addition of a differentiator to the decoder so compensating for the extra integrator at the encoder's input. As the integrator and differentiator in the decoder are identical they can be removed, making the decoder consist of only a low-pass filter. A further simplification of the system is possible because the two integrators in the encoder can be replaced by one integrator. This results in the arrangement shown in Figure A1.4. Repositioning the components of the d.m. to obtain a d.s.m. results in some performance changes.

A1.5.2 Slope Overload

The slope overload condition can again be calculated. Considering the d.s.m. as a d.m. preceded by an integrator the slope overload point can be calculated in a similar way to d.m.

The input applied to the d.m. will be the integral of the input signal:-

$$\int x_t \, dt = \frac{A}{w_s} \cdot \cos w_s t \qquad \text{A1.10}$$

The maximum slope of the input to the d.m. will now be given by:-

$$\frac{dx_t}{dt} = A \sin(w_s t)\Big|_{max} = A$$

so

$$\frac{dx_t}{dt} = A \sin w_s t$$

hence

$$\left.\frac{dx_t}{dt}\right|_{max} = A \qquad \text{A1.11}$$

Thus the slope overload condition will be given by:-

$$A_{max} = \sigma f_m \qquad \text{A1.12}$$

which is independent of the input signal frequency.

A1.5.3 Encoding Threshold

The minimum signal that a d.s.m. can encode will be the integral of that for a d.m., so:-

$$\frac{\sigma}{2} \sin w_s t = \int A_{min} \sin w_s t \, dt = \frac{A_{min}}{w_s} \sin (w_s - \frac{\pi}{2}) \qquad \text{A1.13}$$

after equating the constants on both sides:-

$$A_{min} = \pi \sigma f_s \qquad \text{A1.14}$$

The minimum encoding threshold of d.s.m. is inversely proportional to the signal frequency.

A1.5.4 Dynamic Range

The ratio of A_{max} to A_{min} as defined by equations A1.12 and A1.14 gives the dynamic range (D) of the d.s.m.

$$D = \frac{f_m}{\pi f_s} \qquad \text{A1.15}$$

This is the same result as for d.m.

A1.5.5 Signal to Noise

In exchange for a flat amplitude/frequency characteristic, the

removal of the integrator in the d.s.m. decoder causes the spectral density of the output noise to rise by 6 dB/octave. The power transfer function of an integrator is:-

$$\frac{1}{(2\pi f)^2} \qquad \text{A1.16}$$

this modification of the noise spectrum when considered over the band of interest ($0\text{-}f_c$) modifies the S/N equation of a d.m. to:-

$$S/N = \frac{3}{8\pi^2 Kq}\left(\frac{f_m}{f_c}\right) \qquad \text{A1.17}$$

The S/N in linear d.s.m. is independent of the input frequency unlike d.m.

APPENDIX 1

References

A1.1 Deloraine, E.M., Van Mierlo, S. and Derjavitch, B., French Patent 932,140, August 10th, 1946.

A1.2 French Patent specification, No. 987.238, 22nd May 1948,

A1.3 Delta Modulation Systems, R. Steele, Pentech Press, London.

A1.4 O'Neal, J.B., Delta Modulation Quantizing Noise, Analytical and Computer Simulation Results for Gaussian and Television input Signals; Bell Systems Tech. J., 1966, XLV 1 pp. 117-141.

A1.5 Johnson, F.B., Calculating Delta Modulator Performance, IEEL Trans.Audio and Electroacoustics, 1968, AU-16, pp.121-129.

A1.6 Inose, H. and Yasoda, Y., "A Unity Bit Coding by Negative Feedback", Proc. IEEE, Nov, 1963, pp, 1524-1535,

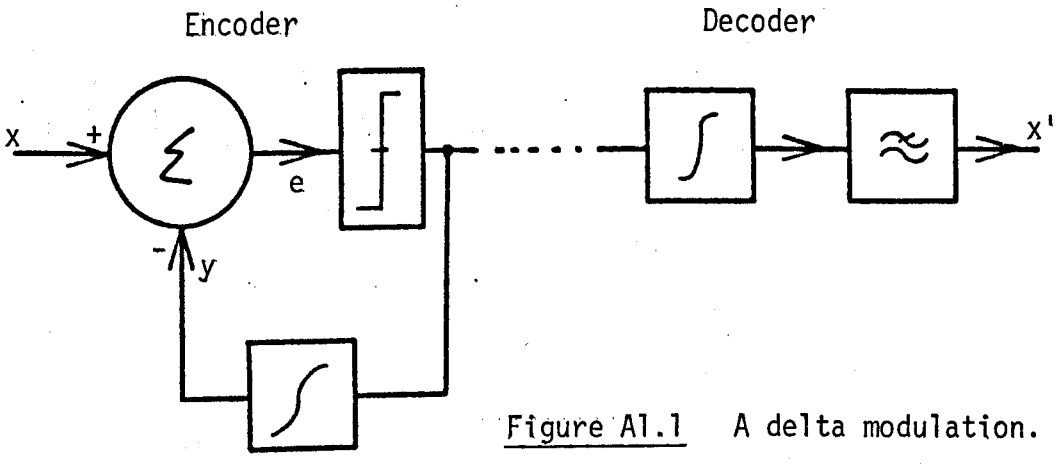


Figure A1.1 A delta modulation.

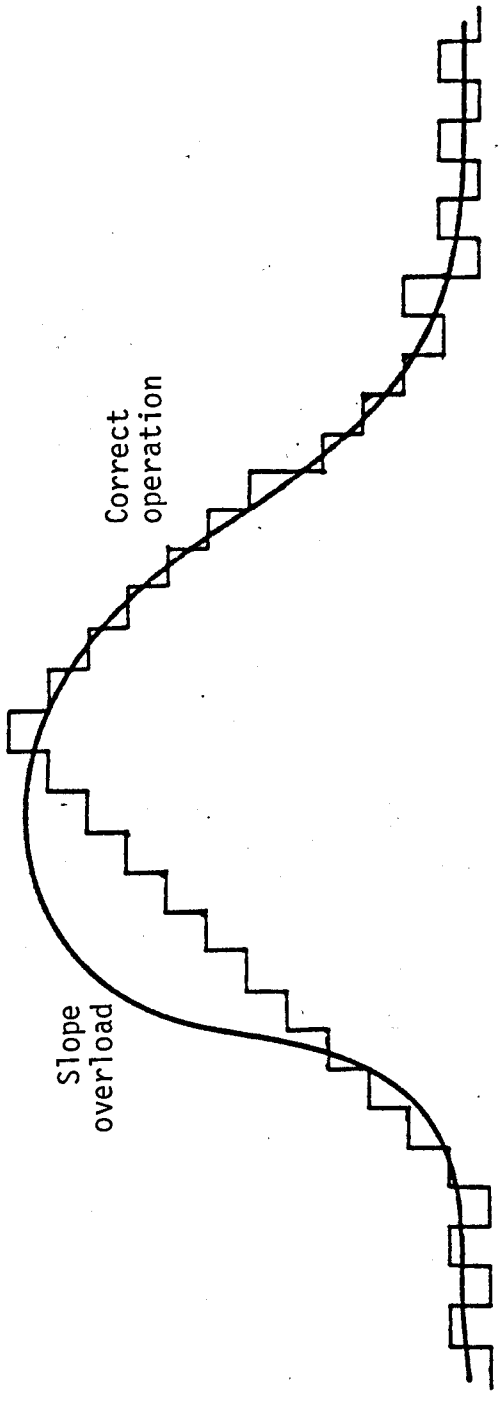


Figure A1.2 Operation of a delta modulator.

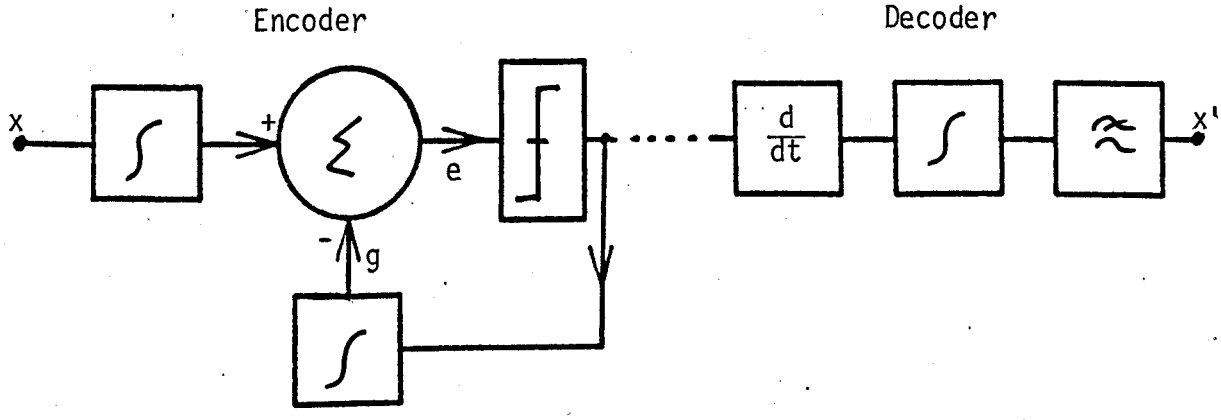


Figure A1.3 Conversion of a d.m. into a d.s.m.

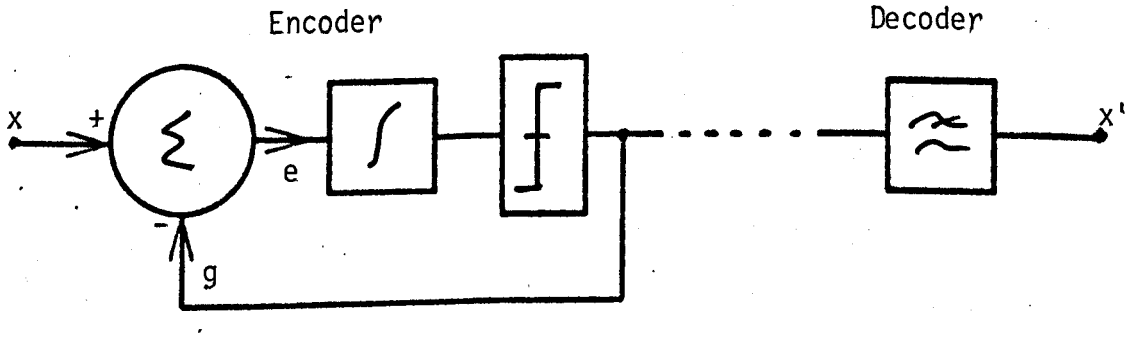


Figure A1.4 Simplified delta modulator.

APPENDIX 2

Measurement Techniques on D/A Converters

This Appendix discusses the measurements taken to assess the performance of the D/A converters described in the main report.

The first section outlines the tests available for quantifying a sound system's performance and discusses their success when compared with subjective measurements. At the end of this section some practical constraints are discussed which limit the type of tests which can be carried out on high quality D/A converters.

Details of the tests used are given in the second section.

The final section describes the relevant constructional details of the test apparatus and summarises the equipment's performance.

A2.1.1 Assessing the Performance of Audio Systems

Techniques for evaluating the quality of an audio system in the laboratory are based on analytical measurements which assign numbers to different kinds of degradation. The correlation between the measured and perceived degradation of a system is difficult to determine, perceived degradation is often very specific, whereas measurement techniques need to be general. Historically, concepts like signal to noise (S/N) and total harmonic distortion (T.H.D.) give a good estimate of a system's dynamic range and linearity. However, these do not take account of sudden changes in noise which can occur as the signal level changes, or the type of harmonic distortion produced. In an attempt to improve the subjective assessment of audio equipment by measurements, various new definitions of S/N and T.H.D. have been developed (Ref. A2.1). New measurements, such as inter-

modulation distortion, have also been introduced. Unfortunately the digital audio profession has not yet developed a well defined testing and measurement system. This has resulted in experimenters using their own definitions of accepted terms, such as S/N. Ways of improving the T.H.D. tests have been suggested by various authors (Refs. A2.2, A2.3). These methods weight the harmonic distortion products produced by a system and propose that increased account should be taken of the amplitude of high order harmonics since these are subjectively more objectional. The B.B.C. have devised many studies, comparing the subjective performance of a system with analytical measurements (Refs. A2.4, A2.5, A2.6). The suitability of these techniques for D/A converters is discussed in the following section.

A2.1.2 Specific Measurements on D/A Converters

A major problem in developing test procedures for D/A converters is in obtaining the required test signals in digital form. The conventional approach requires an A/D converter to produce digital signals from an analogue signal source. These signals are then applied to the D/A converter under test. To enable this system to function satisfactorily the A/D converter must be capable of producing an error free digital output. This arrangement is shown in Figure A2.1. The specification of such a converter, suitable for testing a 14-bit high quality D/A converter is at the limit of current technology. To avoid problems separating any noise introduced by the A/D converter from that produced by the D/A converter under test, an alternative system is proposed. This system is shown in Figure A2.2. The required test signals are synthesised mathematically and a set of digital samples produced. These samples are then stored in the memory of a microprocessor (μP) and output as required at the appropriate sample rate. These synthetic test signals are attractive, since a given test sequence can be repeated precisely for as long as required. Further, no encoding

process is involved, so the test signals are, to that extent, governed by the accuracy of the digital code used. There are practical limitations to this technique. The test signals which can be stored in memory are limited to periodic signals, since the storage requirements of such signals can be reduced to one complete cycle.

To enable subjective tests to be made, and provide a reference D/A converter, a 16-bit high quality A/D and D/A codec was developed. This codec was constructed from purpose-built professional A/D and D/A units and combined with the required sample and hold and filters to produce a complete digital system. The completed codec was found to perform as an ideal 14-bit P.C.M. system. Its performance is fully documented in Section A2.3.2.

Investigations have shown that the degradation in signal quality resulting from using a D.S.M. as a D/A converter can be categorised into three main forms; these can be generalised as:-

1. Encoding noise
2. Harmonic distortion
3. Program modulated noise

The encoding noise is produced by the D.S.M. and is random in nature extending over the whole message band. It consists of the quantization noise contained in the original P.C.M. signal and additional quantization noise produced by the encoder's quantiser.

Peaks of noise occur at intervals harmonically related to the modulating frequency. This harmonic distortion occurs mainly at low harmonics. Most of the harmonic distortion produced by the modulation system described in Chapters 2 and 4 is produced by the output circuitry and is confined to high signal levels. Since the residual error encoder discussed in Chapter 3 produces a unique output sequence for every input level its spectrum consists of peaks of noise which are all harmonically

spaced.

The most difficult form of noise to quantify is program modulated noise. The amplitude of this noise is dependent on the level of input signal and so can only be experienced subjectively on selected extracts of program material, selected passages of solo piano music have been found particularly suitable for assessing program modulated noise.

To quantify these noise signals, thus enabling D/A converters to be compared, three tests have been developed. Any single test does not accurately describe the system, but the combination of all three gives sufficient information to enable comparisons with other systems to be made.

These tests are:-

1. Measurement of the variation of signal to noise ratio over the complete range of input signal levels.
2. Measurement of the power in each harmonic over the message band.
3. Assessment of the dynamic performance of the converter using subjective measurements.

The frequency response of each system is not included in these measurements since no variation between different converters occurs. The ratio of peak signal power to noise produced with no input signal (known as the idle channel noise) was always included in the measurement of signal to noise. Details of each test are given in the next section to enable comparisons with other methods to be made.

A2.2.1 Measurements of Signal to Noise Ratio

The definition of signal to noise (S/N) used is "the ratio, expressed in dB, of the R.M.S. signal input to the R.M.S. noise power produced in the message band". The test apparatus used is shown in the

block diagram, Figure A2.3. The μP is used to produce an 125 Hz sinusoidal signal, which can be varied in amplitude. This is applied to the converter under test. At all times 0 dB of signal is defined as the peak signal which can be encoded without overload. Measurements are then taken at 3 dB increments over the available dynamic range of the converter under test. The output of this converter is band limited by a low-pass filter with a cut off frequency of 15 KHz. The filtered output can then be applied directly to a twin-tee notch filter and R.M.S. power metre, or first filtered by a 500 Hz high pass filter. To give a more accurate assessment of the encoding noise the noise power is taken when the high pass filter is in circuit, this removes the first three harmonics of the input signal leaving the noise in the band 500 Hz - 15 KHz. This approach is more flexible, since at high signal levels the harmonic distortion contained in the first three harmonics can dominate the noise power measurement. The S/N results including the harmonic distortion can be calculated if desired, by including the harmonic analysis results. At input signal levels less than -9 dB no significant difference is observed between the two methods since the harmonic distortion falls below the encoding noise floor.

A2.2.2 Measurement of the Harmonic Noise Levels

The power contained in each harmonic of the signal frequency is measured using a spectrum-analyser. It is only practical to measure the harmonic distortion at high signal levels, before the harmonics become masked by the general encoding noise. The required test signal is generated using the μP. To increase the dynamic range of the available spectrum analyser above 80 dB a high-pass filter can be selected, as shown in Figure A2.4, to attenuate the fundamental frequency by 60 dB. This enables the sensitivity of the spectrum analyser to be increased without overloading. Measurements down to -100 dB have successfully been made using

this arrangement. Tabulating all the individual harmonic levels enables the total harmonic distortion to be calculated and also indicates where significant harmonic distortion occurs.

A2.2.3 Subjective Measurement

These measurements, by their nature, are difficult to quantify. The program, material used must be chosen with care to avoid masking the noise under examination. Solo piano scales have been found to be the most critical test signals. The program modulated noise can then be clearly heard as a sawing noise following the amplitude of individual notes. Unfortunately recorded test signals, either on tape or digitally mastered records produce their own noise which cannot be disassociated from the coder under test. To avoid this, an electronic test signal generator was constructed. Such a system was developed by the B.B.C. (Ref. A2.7) for this application. This system was duplicated and used for the subjective tests.

This system produces a test signal which varies in level in a predictable and repeatable manner. The type of signal produced is sufficiently different in character to avoid masking the impairment under test, it sounds like a series of piano notes.

Figure A2.5 shows the functional components of the "electronic gong" (Ref. A2.7). The apparatus comprises essentially of four tone generators whose outputs are switched, in a pre-set pattern at a pre-set rate, to an envelope shaper and thence, through low-pass and high-pass filters, to an output amplifier. The envelope shaper causes the signal to have a smooth short rising edge and a long decaying edge. This is shown in Figure A2.6.

The use of this electronic gong is illustrated in Figure A2.7. The digital test signal is derived by using the reference A/D converter to encode the output of the gong, or a live program source as required. The filtered output of the D/A converter under test is then applied to a

power amplifier which drives a pair of monitor loudspeakers. A particularly stringent test can be made by adjusting the gong to provide a series of single notes which is then applied to the converter under test. The output signal is then filtered, to remove the fundamental component of the gong; what is left behind consists only of unwanted noise and distortion introduced by the equipment.

The amount of program modulated noise was estimated by the author and his colleagues when compared with the reference coder.

A2.3.1 Generation of the Computer Test Signals

This section describes the construction of a digital signal generator under the control of a μP. The choice of μP is governed by its operating speed and the accuracy of samples required. The advent of 16 bit μP's have made it possible to output a complete 16-bit word in one operation. Suitable development kits which combine a central processor with all the required peripheral hardware and a simple operating system are now available, such a system, an SDK-86 development system (Ref. A2,8), produced by Intel which uses the 16 bit 8086 μP was selected as the basis of the digital signal generator. A block diagram of this development system is given in Figure A2,8. This system contains all the components required. The speed of a clock cycle is 200 nS this constrains the amount of processing which can be undertaken between outputing successive words at a sample rate of 32 KHz. To reduce the amount of processing required the program which controls the output data is written in two parts.

A flow chart of the program is given in Figure A2.9. The original data, stored in the first block of memory represents a peak amplitude sine-wave at the lowest frequency required. The number of samples required can be calculated using Equation A2.1

$$\text{number of samples} = \frac{f_s}{f_w} \qquad \begin{aligned} f_s &= \text{sample frequency} \\ f_w &= \text{signal frequency} \end{aligned} \qquad \text{A2,1}$$

provided the signal frequency is a sub-multiple of the sampling frequency an integer number of samples will be required. Part 1 of the program calculates the required output signal level, and frequency selected by the user from the original data store. The prototype unit used could produce output levels in 3 dB steps at frequencies of 125 Hz, 500 Hz, 1 KHz, 2 KHz, 4 KHz and 8 KHz. The second block of memory is filled with new data sequentially. Each sample is first selected from the original data store, it is then multiplied by a constant to produce the required attenuated sample and placed in the second memory block. The frequency of the required signal is determined by the choice of samples taken from the original block. The lowest frequency output signal will require all the data samples. Higher frequency are generated by jumping over unwanted intermediate samples. Generating a second block of data removes the need to calculate the new samples within the required output sampling period. When all the samples are processed the program jumps to the second part of the program.

With all the required data stored in R.A.M. the second part of the program can be simple and fast. This program simply transfers successive words of data from memory to the output port. This transfer of data is controlled by an interrupt line which is interfaced to the sample frequency clock, this ensures the μP is synchronized. When all the data contained in the second memory block has been sequentially outputed a complete cycle of test data has been produced, so the program jumps back to the start of the memory block and the process is repeated. The transfer of data continues in this manner indefinitely, unless the μP is reset. Then a new set of data can be specified and the program re-run.

The original block of data was calculated by computer, where a single cycle of signal was sampled, then quantized to the required accuracy, using integer arithmetic. These samples were then converted into hexadecimal words and outputed to paper tape. The control program and

associated data are conveniently stored on paper tape and loaded into the μP as required.

This complete system has proven a robust and accurate P.C.M. signal generator which will provide up to 16-bit P.C.M. at sample rates of less than 64 KHz. Various versions of the programs were written to add D.C. and A.C. offsets to the P.C.M. data for the investigations discussed in Chapter 2. The range of test signals which can be produced in this manner is limited only by the amount of memory available.

A2.3.2 The Development of a Reference Codec

This section briefly describes the construction and specification of a 16-bit A/D and D/A codec which could be used as a reference to compare the performance of the D/A converters described in the main report. This codec was constructed by combining a number of ready made units. It has four major components.

The A/D converter consists of a 16-bit high accuracy hybrid circuit produced by Zeltex (Ref. A2.9). This converter has a claimed accuracy of ±0.0015% and a conversion speed of 20 μs. A 16-bit hybrid D/A converter produced by Burr-Brown (Ref.A2.10) provides D/A convertion. This converter settles in less than 10 μs with a maximum non-linearity of ±0.003%. These units were combined with a high quality sample and hold circuit, (Ref. A2.11) a de-glitcher circuit (Ref. A2.12) and associated control logic on a double sided P.C.B.. A block diagram of the complete system is given in Figure A2.10. Shown in this diagram are an additional set of buffers on the output of the A/D, these were included to protect the converter from accidental damage. The input to the D/A is multiplexed to enable direct connection to the A/D for testing or connection to an external digital signal. The system was designed to operate at a sample rate of 32 KHz and be synchronized to an external clock.

Extensive testing of this codec indicated that it could provide the required 14-bit performance, full 16-bit performance could not be

obtained. A summary of each component's performance is given in Figures A2.11-A2.13. These results show the signal to noise ratio and harmonic distortion introduced at each stage.

A2.3.3 Specification of the Test Equipment

It is considered necessary to provide the reader with a summary of the test equipment used for all the measurements given in this report. Although the test apparatus has been discussed in previous sections of this appendix, it is convenient to summarise all the test equipment, and its interconnections in one diagram, Figure A2.14. A comprehensive list of the equipment is included at the end of this section in Table A2. A photograph of the assembled system is given in Figure A2.15 for reference.

QUAD 44	Pre-amplifier
QUAD 405	Power amplifier
SPENDOR BC1	Monitor loudspeaker
REVOX A77	Tape recorder
ORTOFON M20FL	Pick-up cartridge
RADFORD Series 4	Distortion measuring set
RADFORD L005	Low distortion oscillator
TEKTRONIX 7L5	Spectrum analyser

Table A2

List of test equipment

APPENDIX 2

References

A2.1 Geddes, W.K.E., 1968, The Assessment of Noise in Audio-frequency Circuits, B.B.C. Research Department.

A2.2 Shorter, D.E.L., 1950, The Influence of High-order Products on Non-linear Distortion, Electron Engng, 1950, 22, 4, p.152-3.

A2.3 Wigan, E.R., 1961, New Distortion Criterion, Electron Technol, 1961, 38, 4+5 pp.128-137, 163, 174.

A2.4 Belcher, R.A., 1974, An Experimental Investigation of Test-noise Signals for the Measurement of Non-linear Distortion of Sound Signals, B.B.C. Research Department Report, RD 1974/2.

A2.5 Belcher, R.A., 1976, Audio Non-linearity : A Comb-filter Method for Measuring Distortion, B.B.C. Research Department Report RD 1976/12.

A2.6 Belcher, R.A. 1977, Audio Non-linearity : An Initial Appraisal of a Double Comb-filter Method of Measurement, B.B.C, Research Department Report EL 135.

A2.7 Manson, W.I. and Reid, D.F., Two Audio Test Signal Generators for Assessing Program Modulated Noise in Digital Compandors, B.B.C. Research Department Report, EL 125.

A2.8 MCS-86 Users Manual Intel Corporation.

A2.9 Zeltex SAD700/ZAD7400 Data Sheet, 1980.

A2.10 Burr-Brown DAC71/DAC72 Data Sheet, 1978.

A2.11 B.B.C. Research Department, private communication.

A2.12 Analog Devices A1-2425 Data Sheet, 1978.

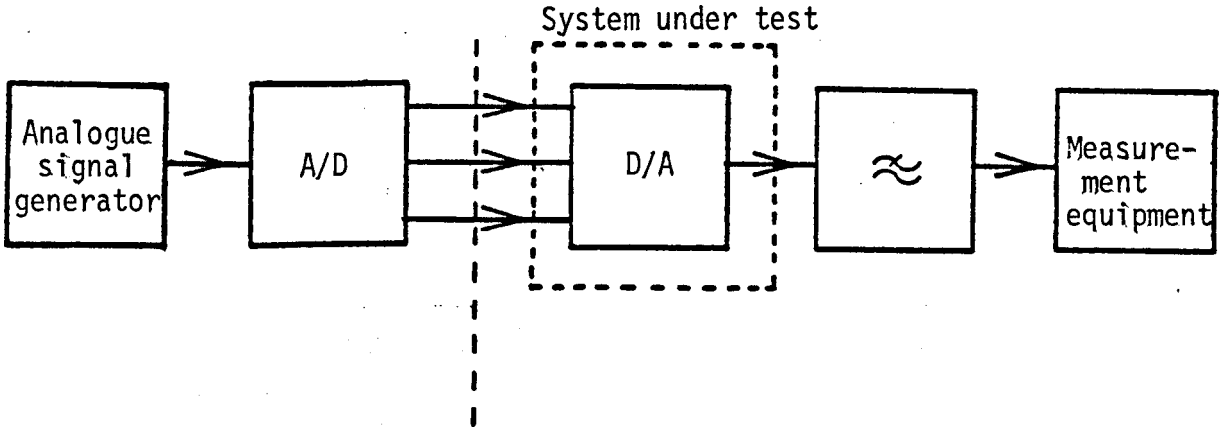


Figure A2.1 Conversion of an analogue signal for testing a D/A.

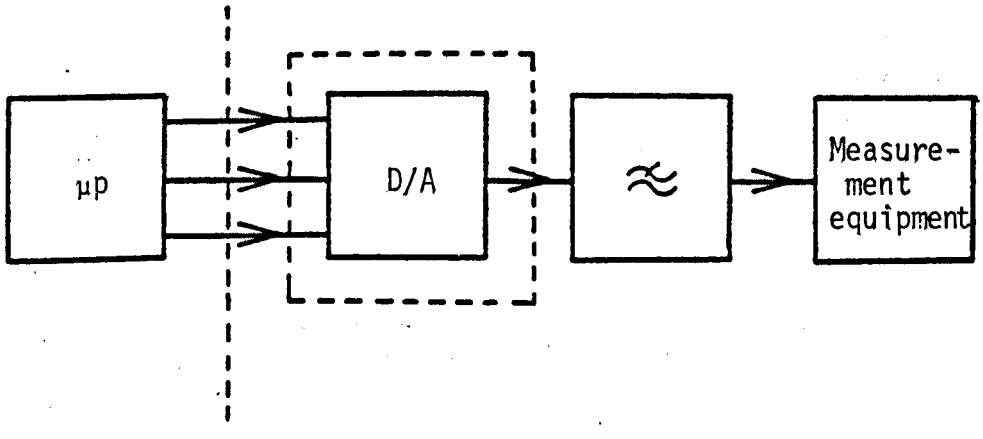


Figure A2.2 Use of a µp to produce test signals.

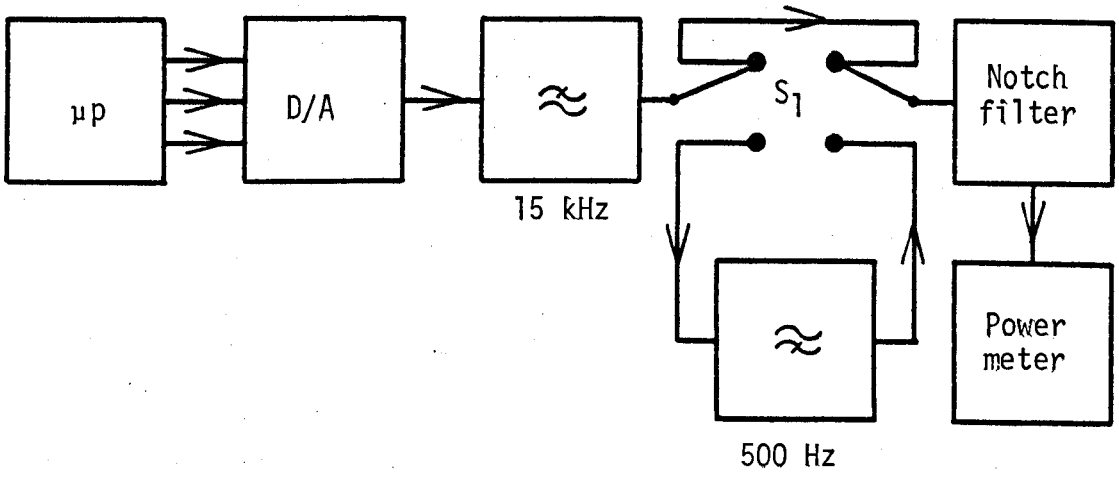


Figure A2.3 Equipment for measuring S/N ratio.

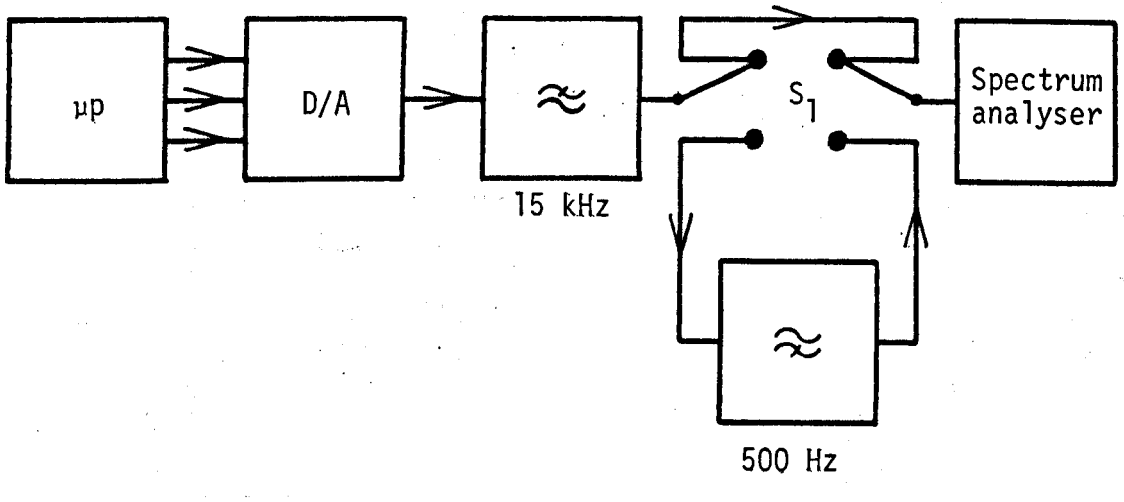


Figure A2.4 Equipment for measuring the harmonic distortion.

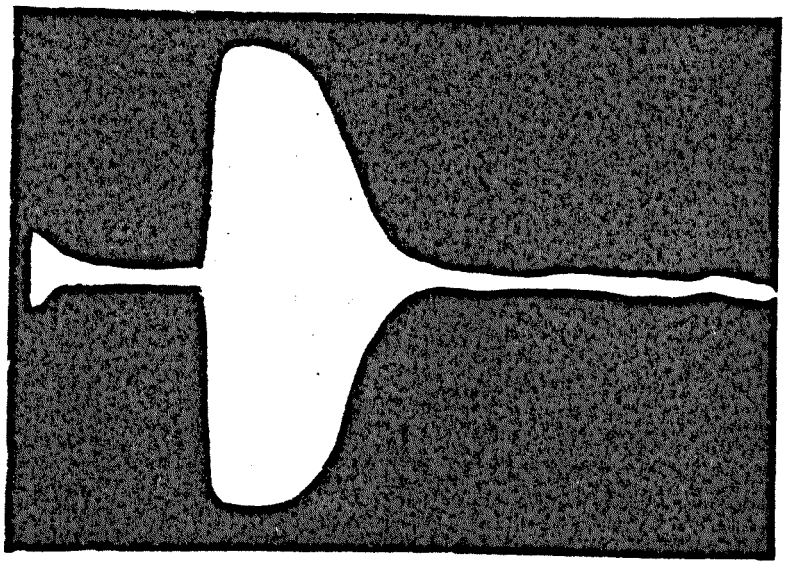


Figure A2.6 Resulting output signal.

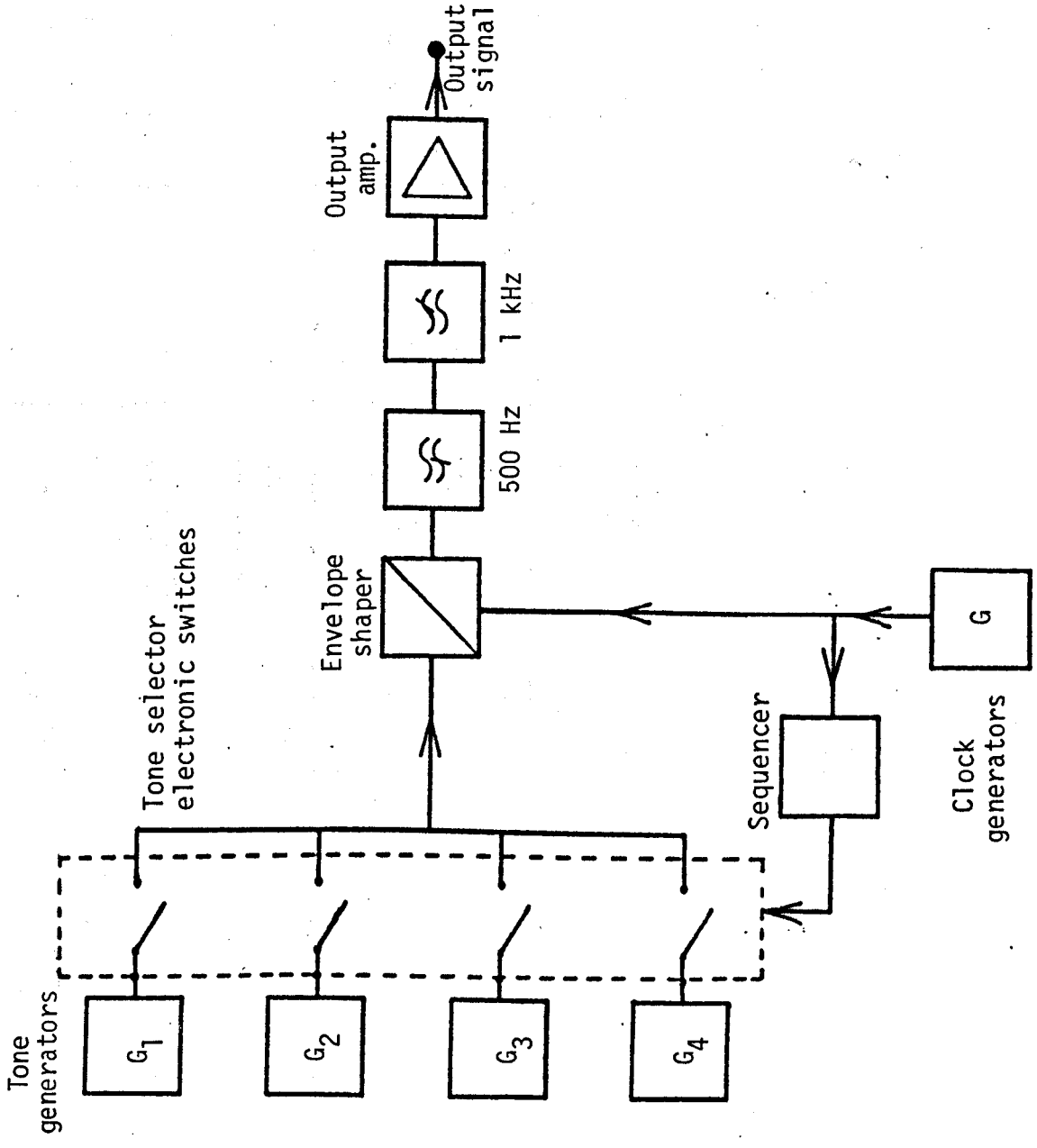


Figure A2.5 Electronic gong's functional diagram.

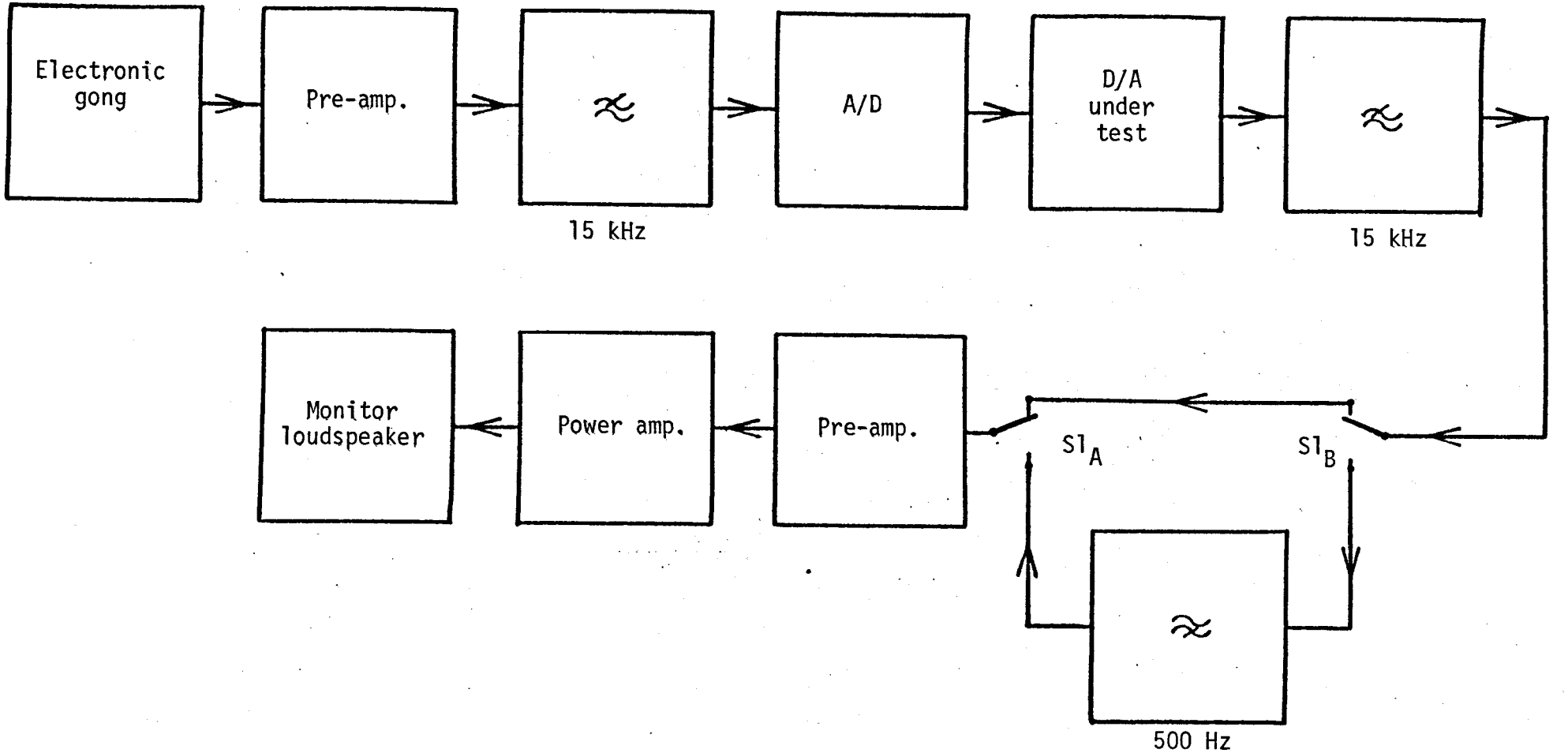


Figure A2.7 The use of the electronic gong.

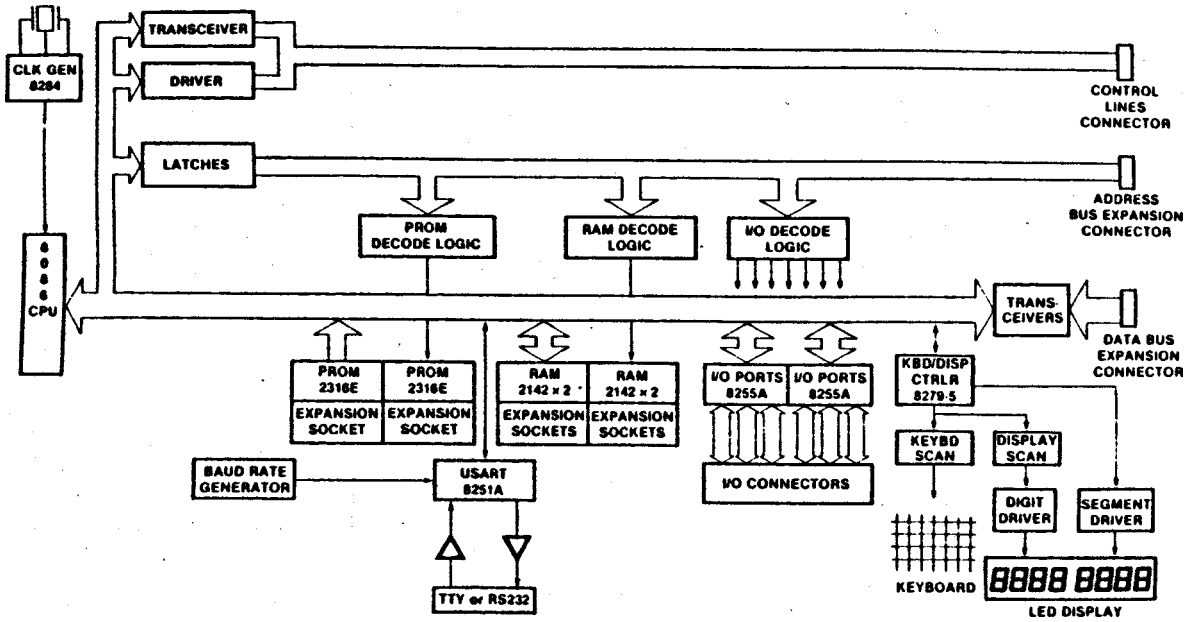


Figure A2.8 **SDK-86 System Design Kit Functional Block Diagram**

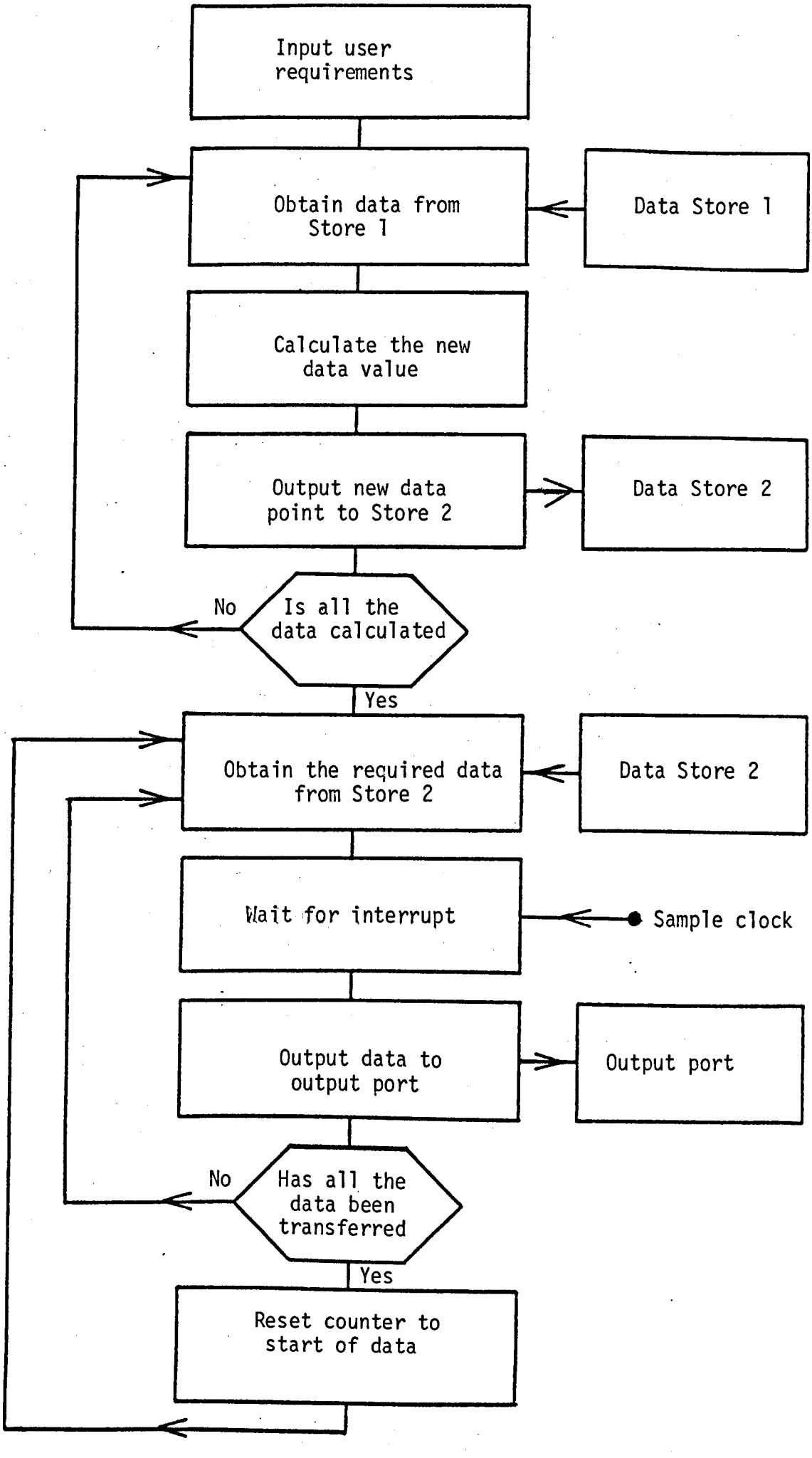


Figure A2.9 Test program's flow chart.

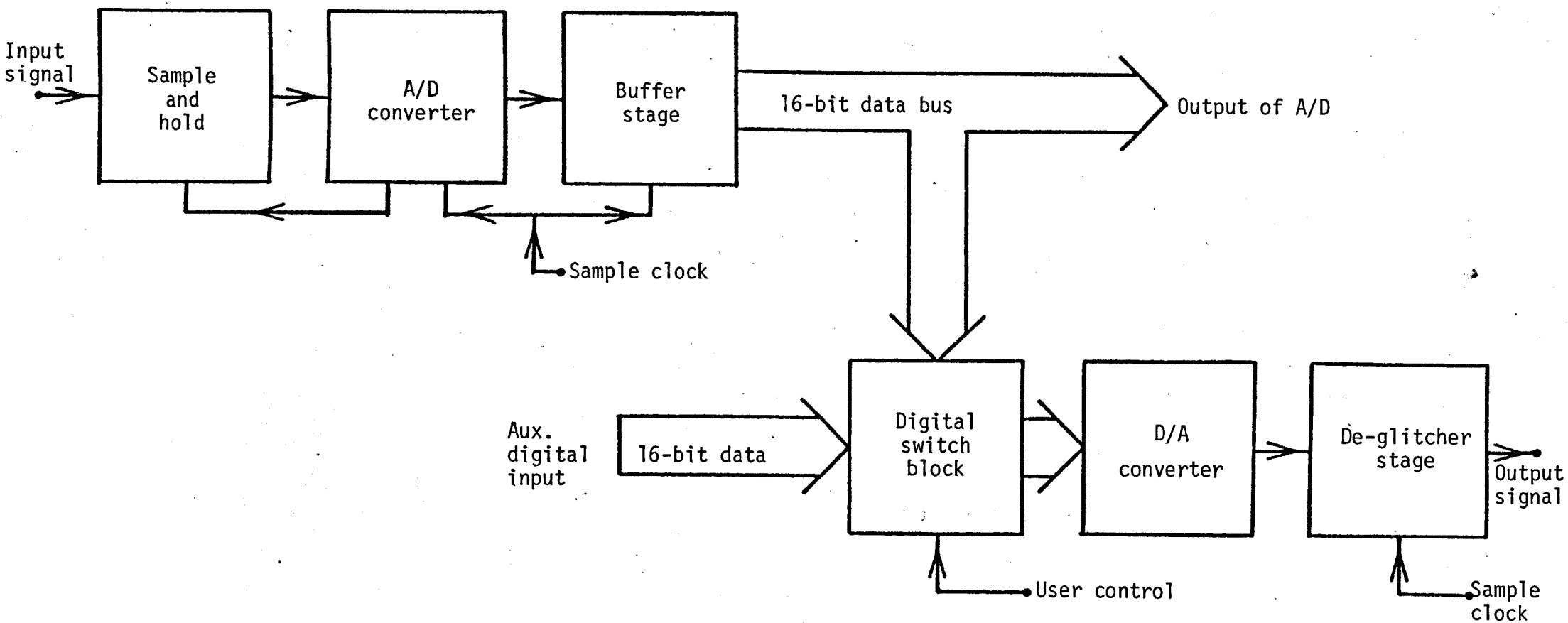


Figure A2.10 Block diagram of the reference codec.

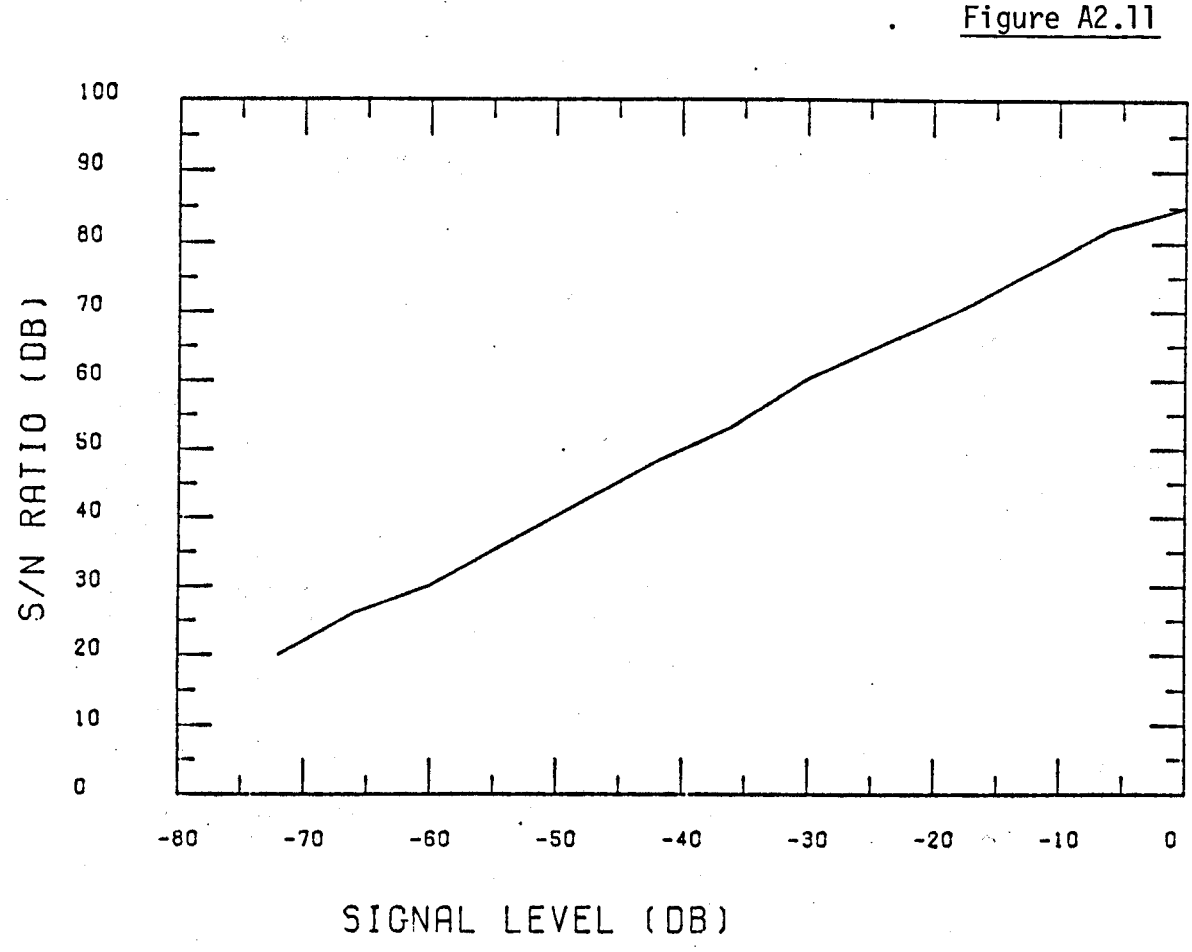


Figure A2.11

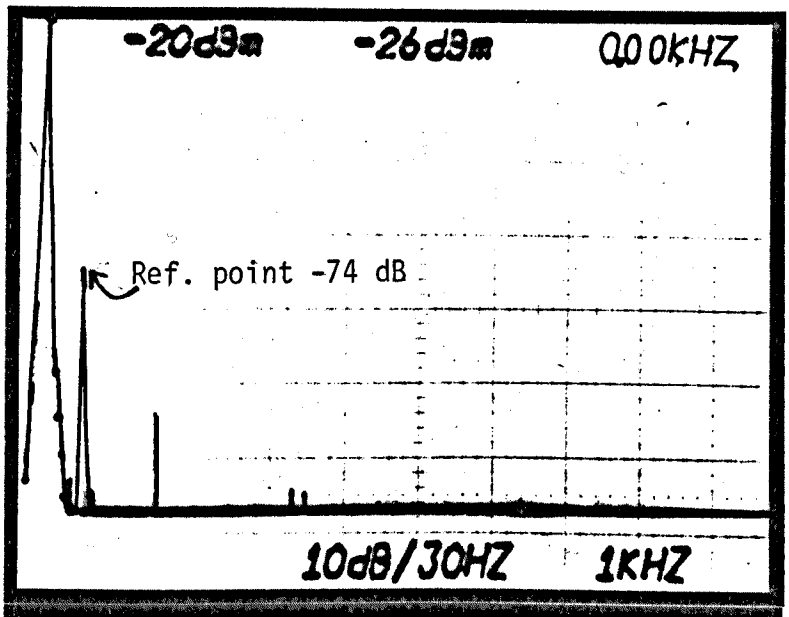


Figure A2.12a

Spectrum of Sample and Hold with a peak level 500 Hz input signal.

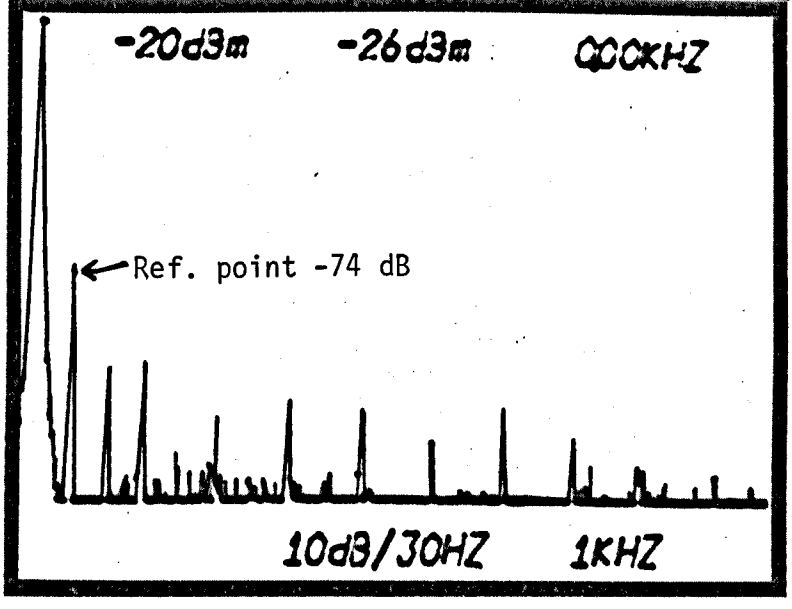


Figure A2.12b

Spectrum produced by A/D - D/A codec with a peak 500 Hz input signal.

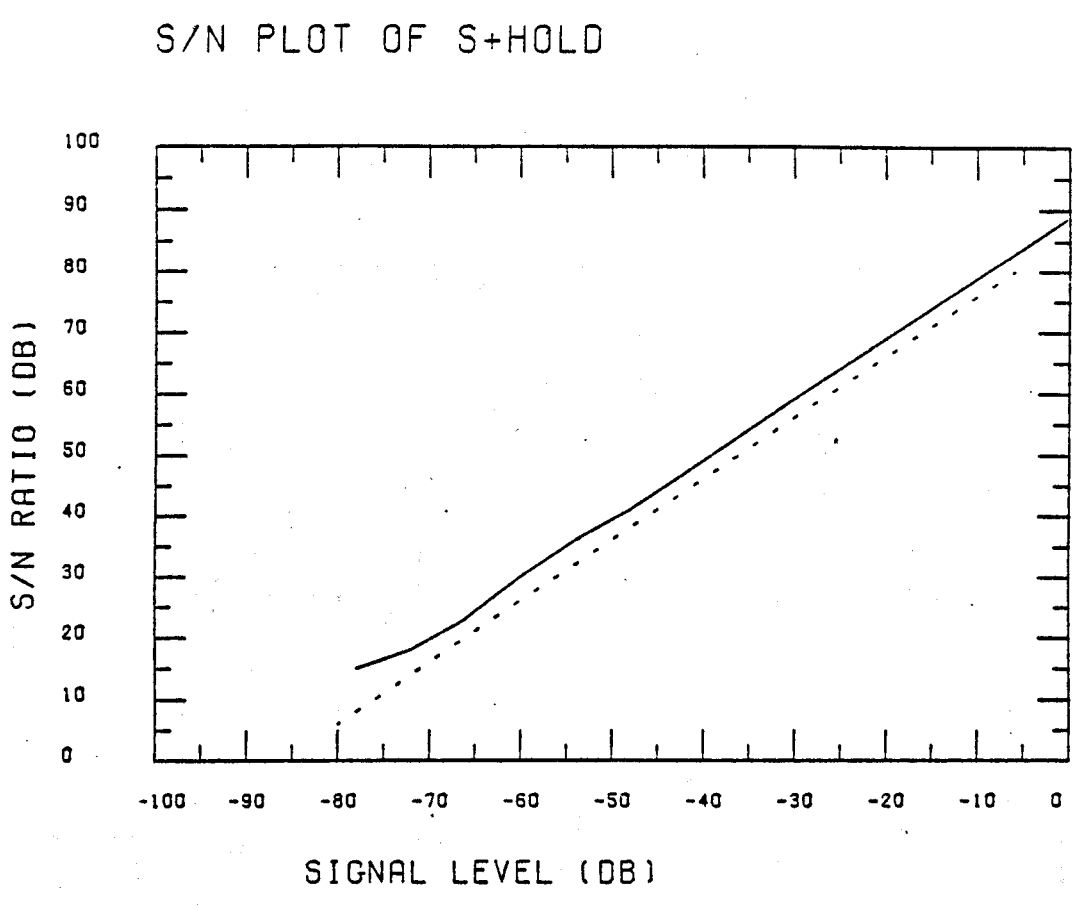


Figure A2.13a

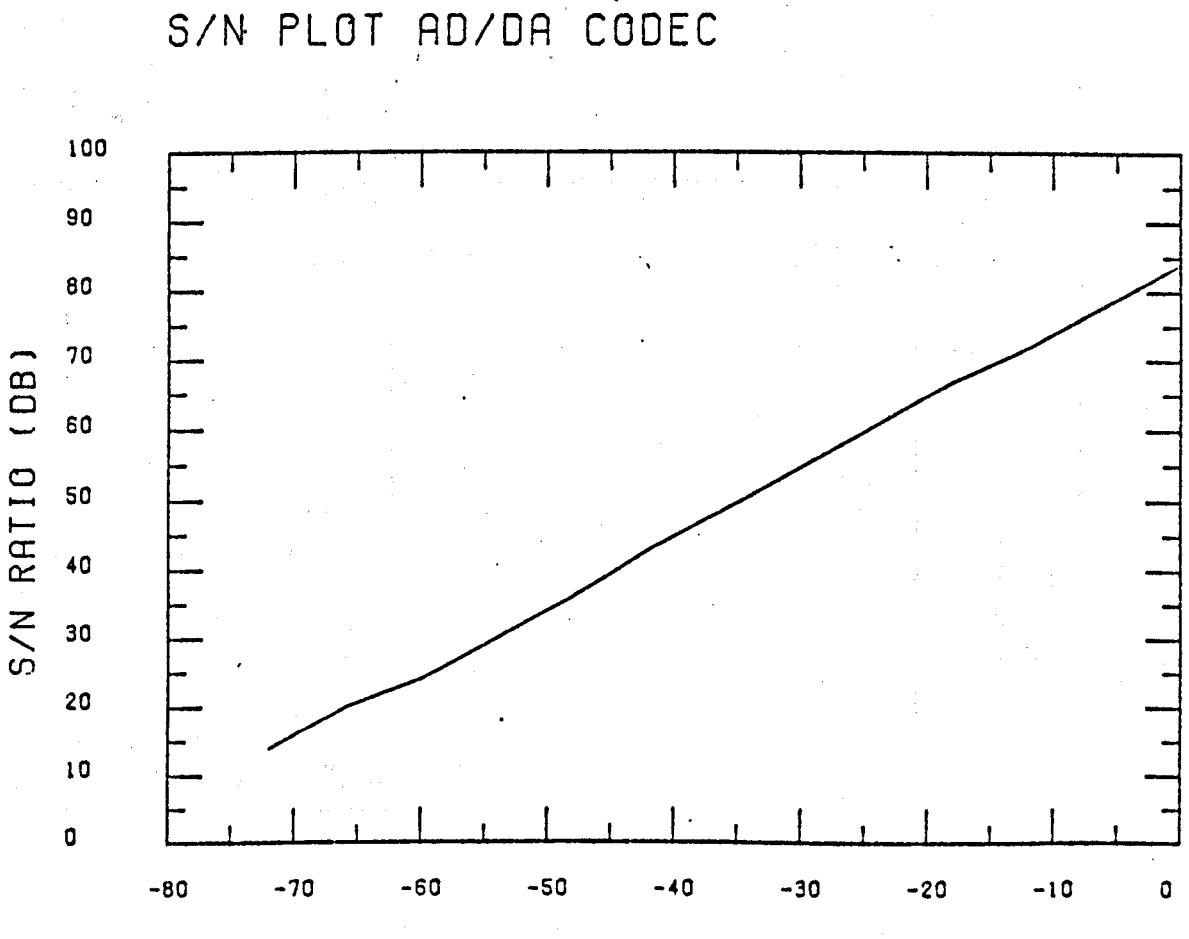


Figure A2.13b

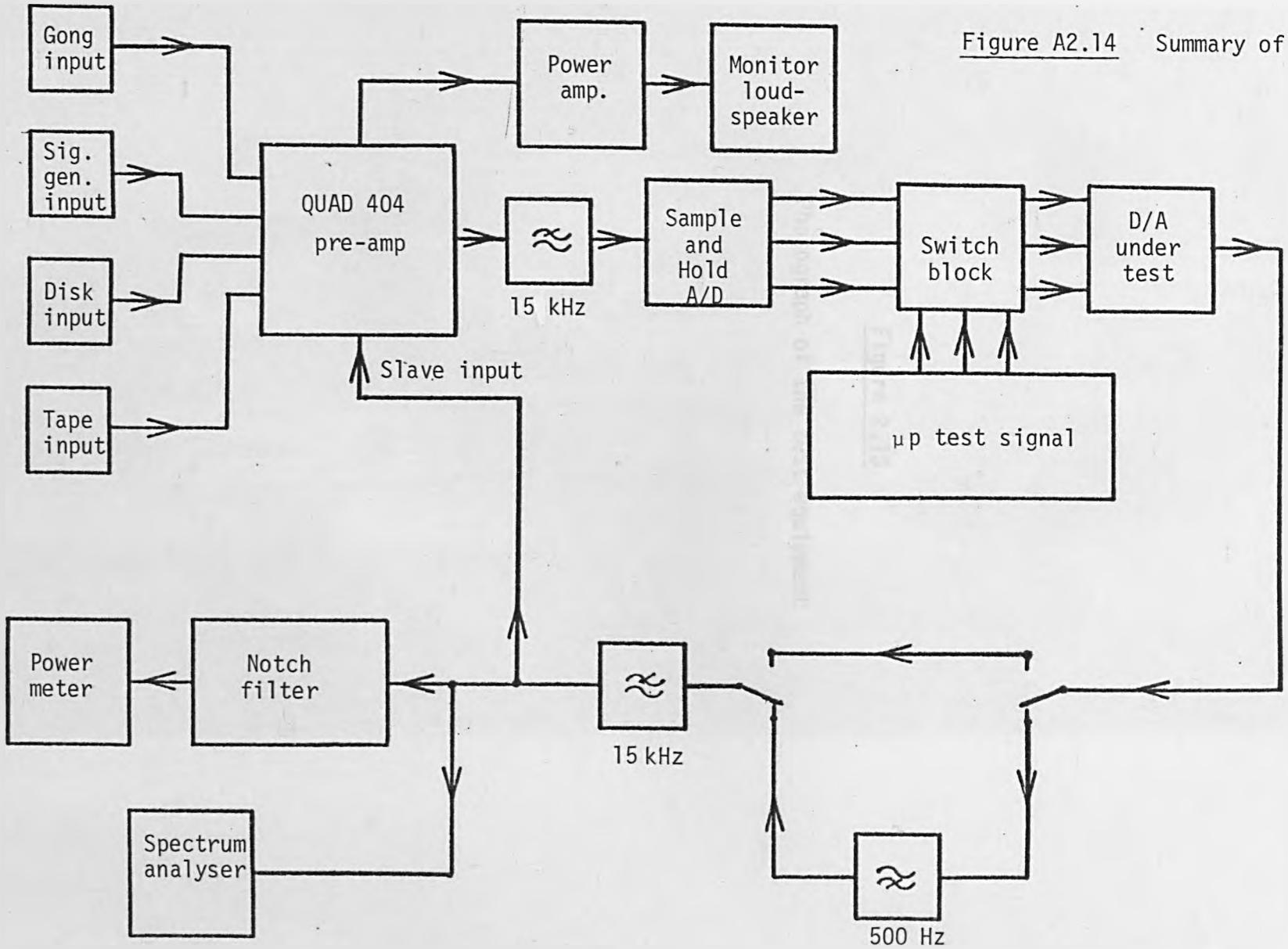
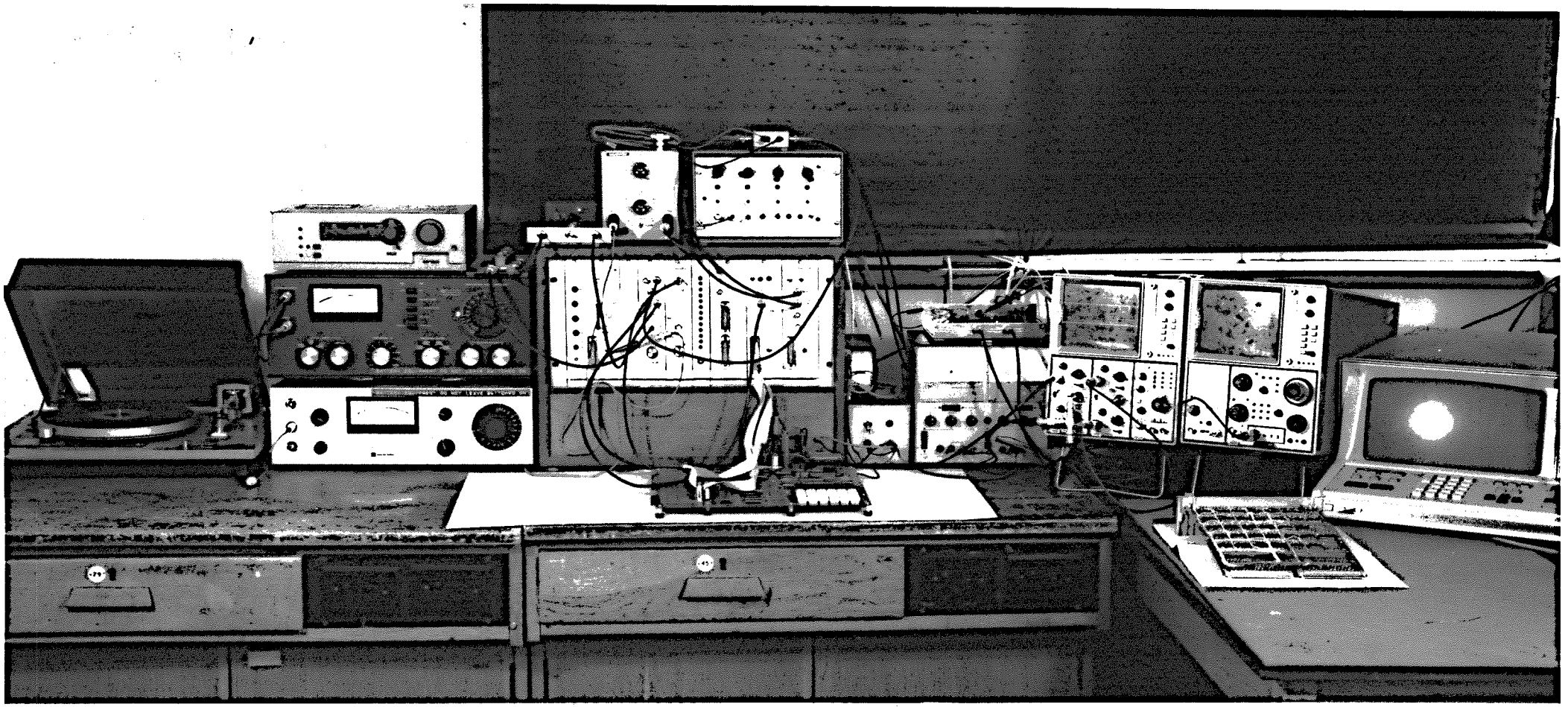
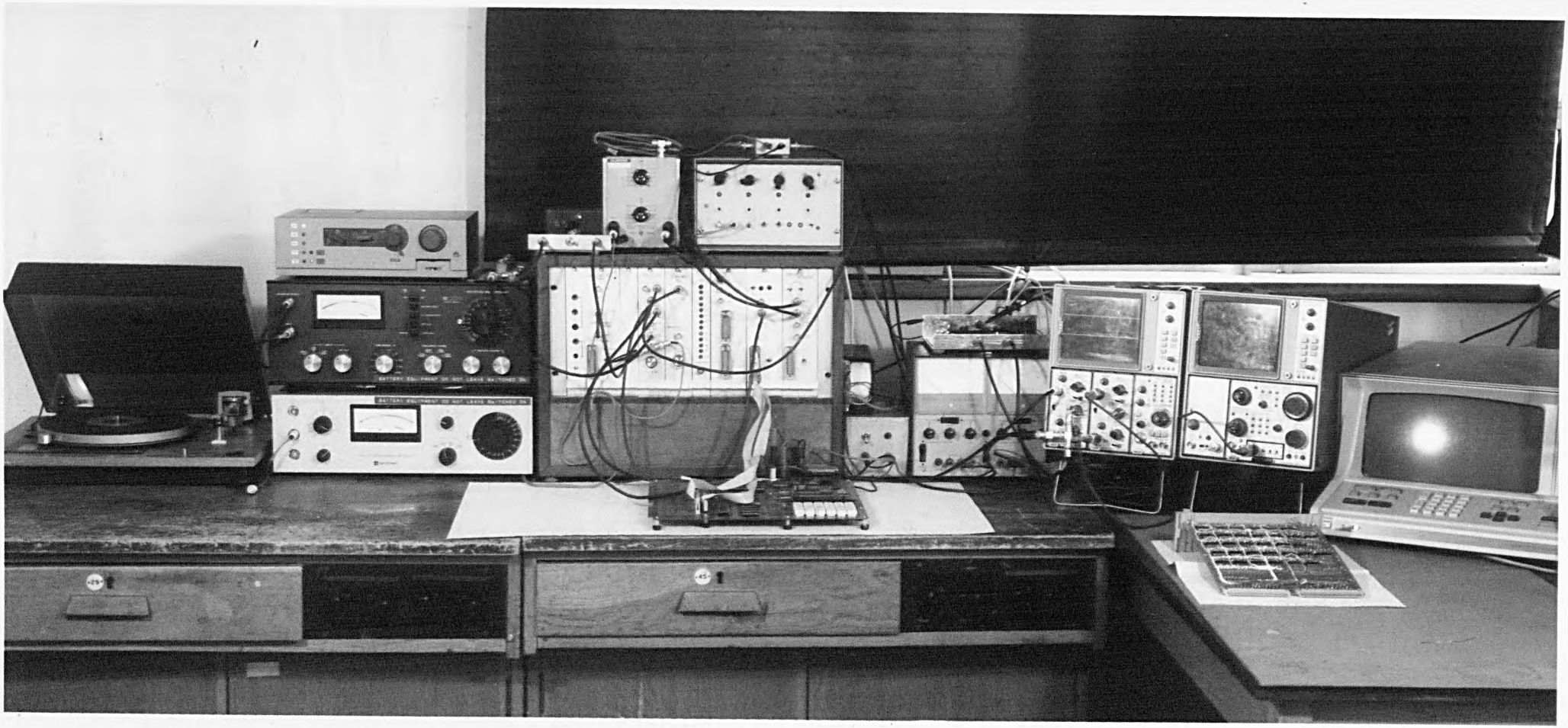


Figure A2.14 Summary of test apparatus.





APPENDIX 3

Constructional Details of the Hardware

This Appendix gives details and circuit diagrams of the converters discussed in the main report. Most of these circuits are self-explanatory although relevant theory and constructional points are included as required.

The first section of this appendix describes the digital circuitry of each coder. All these circuits are constructed using TTL M.S.I. circuits contained on a single circuit card. These cards are designed to plug into the backplane of a racking system, where they receive all the power-supplies and input signals required.

The second section describes the circuit details of the analogue circuitry which is necessary to convert the D.S.M. code, produced by the coders into an analogue signal. These circuits are assembled on a single circuit card contained in the racking system. Additional information on the clock generator, analogue filters, and low-noise amplifiers used in the completed system is included at the end of this appendix. A selection of photographs are given to show how the equipment was constructed.

A3.1.1 The 14-bit First Order Delta Sigma Modulator

This coder is described in Chapter 2. It was designed to encode 14-bit P.C.M. data, at a sampling frequency of 32 KHz, and produce a single bit D.S.M. code. In addition, the clock frequency of this modulator could be changed, as required, up to a maximum of 8 MHz. Extra circuitry was provided on the input to the d.d.s.m. to add the required AC or DC offsets.

The circuit of the d.d.s.m. is shown in Figure A3.1. It consists of three main components. An input buffer, a set of 15 full adders, and a

second set of buffers. The incoming twos complement P.C.M. data is connected to 14 D-type flip-flops which form the input buffer. These re-time the incoming data and hold it constant during its conversion to D.S.M. code. The 14-bit twos complement data is converted into offset binary code, required by the modulator, by inverting its M.S.B. The new data is then connected to the lower 14-bits of a 15-bit accumulator. This 15-bit accumulator is constructed from 15-full adders and 15 D-type flip-flops.

The approximation signal of the d.s.m. is obtained from the M.S.B. of the second set of flip-flops. It is subtracted from the input signal by first inverting it with an inverter gate, before connecting it to the remaining 15^{th} bit of the accumulator. The approximation signal also forms the D.S.M. output. The whole modulator requires 12 integrated circuits equivalent to approximately 630 individual gates. The operating speed of the modulator is determined by the rate the second set of D-type flip-flops is clocked. The maximum operating speed is governed by the settling time of the adders, this occurs at approximately 22 MHz.

The addition of the required offsets is accomplished using the circuit shown in Figure A3.2. The incoming P.C.M. signal input is processed by this circuit before being applied to the digital d.s.m. Initially the P.C.M. input is buffered by 14 D-type flip-flops and then applied to 14 full adders. These adders are used to add the required offset. The level of offset added is determined by connecting the required inputs of the adder to either the "logic 1" or "logic 0" line. These lines remain permanently at logic 1 and logic 0 respectively when a D.C. offset is being applied, but are complemented on alternate input samples when an A.C. offset is added. They are controlled by combinational logic, under the control of the input sample frequency clock. To avoid corruption of the sign-bit by adding an offset ot high level input signals, possible overload is detected by two

Nand gates. These then control a set of logic gates which pre-set the output signal to the maximum or minimum level as required.

A3.1.2 The Error Feed-Forward System

A full circuit of the error feed-forward system is not considered necessary, since it consists of a number of functional blocks which have previously been described. The interconnection of these functional blocks is shown in Figure A3.3. The 14-bit P.C.M. input signal is connected to the input of a d.d.s.m. which is identical to Figure A3.1. The output of this modulator is connected to the digital filter, which produces a 14-bit filtered output signal. This signal is subtracted from the original input signal to produce an error signal. To compensate for the delay introduced by the first modulator and the digital filter the input signal is delayed by a set of D-type flip-flops clocked at the appropriate rate. Subtraction is achieved by adding the digitally filtered data to the complement of the input signal. Scaling of the error signal by K is accomplished by shifting its bit field. The scaled error signal is then applied to a second d.d.s.m. identical to the first.

The circuit of the digital filter is shown in Figure A3.4. The output of this filter (Y(z)) is defined by Equation A3.1.

$$Y(z) = 2\,Y(z) \cdot z^{-1} - Y(z) \cdot z^{-2} + X(z) \cdot z^{-64} - 2X(z) \cdot z^{-128} + X(z) \qquad \text{A3.1}$$

Since the input to this filter (X(z)) can only have two possible values implementation of equation A3.1 can be simplified by combining all the X(z) terms with combinational logic forming $X_s(z)$. Thus the filter hardware need only implement the function described by equation A3.2.

$$Y(z) = 2\,Y(z) \cdot z^{-1} - Y(z) \cdot z^{-2} + X_s(z) \qquad \text{A3.2}$$

The D.S.M. output X(z) which is the input to the filter, is applied to

two 64-bit shift registers to produce $X(z) \cdot z^{-64}$ and $X(z) \cdot z^{-128}$ these two outputs together with the input signal are connected to a combinational logic circuit which produces three bits of data representing $X_s(z)$. In addition the output $X(z) \cdot z^{-64}$ is connected to an extra D-type flip-flops to provide the required delayed D,S,M, 1 output.

The processing of the remaining terms is achieved using two sets of D-type flip-flops and two sets of full adders. The first set of adders combines both $2\ Y(z) \cdot z^{-1}$ and $-Y(z) \cdot z^{-2}$ to produce an intermediate result $Y_1(z)$. This is applied to the second set of adders with $X_s(z)$ to produce the required output $Y(z)$. This output is connected to the first set of D-types whose output forms $Y(z) \cdot z^{-1}$. In turn this is applied to the second set of D-types to produce $Y(z) \cdot z^{-2}$. Multiplication of $Y(z) \cdot z^{-1}$ by two is achieved by shifting its bit-field by one-bit. The term $-Y(z) \cdot z^{-2}$ is generated by using the complement of $Y(z) \cdot z^{-2}$ and adding an extra 1 into the L.S.B. of the first set of adders. All the flip-flops are clocked at the d,d,s,m, clock frequency so the output of the filter is not decimated. Sample rate reduction is achieved by clocking the input buffer stage of the second d,d,s,m, at the required sample rate. The cut-off frequency of the filter is determined by the length of the two single-bit shift registers and is therefore readily changed.

A3.1.3 The Residual Error Encoder

As this converter operated successfully a full circuit diagram is included in Figure A3.5. This circuit consists of two identical 7-bit d.d.s.m. each of which is constructed in a manner identical to that of Figure A3.1. The top seven bits of the input signal are connected to the first encoder and the remaining seven bits of data to the second modulator. The two output signals are produced by the single bit outputs of the two encoders. The whole circuit contains 13 integrated circuits, which is equivalent to approximately 690 separate gates.

A3.1.4 The Second Order Modulator

The circuit details of the second order system are conveniently given by reference to three diagrams. The first diagram, Figure A3.6, shows a functional diagram of the complete system. The notation used in this diagram is used to explain the operation of the input circuitry, shown in Figure A3.8, and the second order modulator, shown in Figure A3.7.

Operation of the second order system is described first. The circuit consists of four major components, two sets of adders and two sets of buffers. The combined feedback signal ($X_F(z)$) which is produced by the combinational logic circuits, when combined with the 14-bit input data, produces a 20-bit word which is connected to one set of inputs of the first set of adders, which consists of 20 full adders. The second input of these adders is connected to the output of the last buffer stage; this adds the signal $-Y(z) \cdot z^{-1}$. The output of this set of adders is connected to one set of inputs on the second set of adders. The bit shifted output of the first buffer stage ($2\ Y(z) \cdot z^{-1}$) forms the other input to these adders. The output of this second set of adders forms the un-quantized output signal Y(z). The quantized single bit output of the modulator is formed by taking the sign-bit of this signal. The feed-forward signal ($Y(z) \cdot z^{-1}$) is obtained by connecting Y(z) to the inputs of the first buffer stage, which consists of 20 D-type flip-flops. Similarly the second feed-forward signal ($Y(z) \cdot z^{-2}$) is obtained by using the second set of 20 flip-flops. All the flip-flops are clocked at the same time by the modulator clock. The maximum frequency of this system is determined by the settling time of all the adders. If standard L.S. TTL is used, the limit is 6 MHz. The complete circuit contains 20 individual integrated circuits which is equivalent to approximately 1600 individual gates.

It was shown in Chapter 4 that the second order modulator went unstable when peak signals were applied. The input circuitry shown in

Figure A3.8 detects these peak signals and limits its output data to the maximum signal which causes no overload.

The input signal is first re-timed by a set of D-type flip-flops. Peak input signals are then detected using the four input Nand gate. If overload is detected, the output of this gate causes the set of gates transmitting the output data to produce the maximum permitted output. When no overload occurs this circuit simply re-times the P.C.M. input data.

A3.2.1 The Differential Output Circuit

The differential output circuit is necessary to correct for the unequal rise and fall times on the output pulses produced by the modulators. The circuit is shown in Figure A3.9. The input to the circuit is the output pulses produced by the converters. This input is applied to a D-type flip-flop. The same signal is then inverted, by an inverting gate, and applied to a second D-type flip-flop. These two flip-flops are clocked by the modulator clock. This arrangement ensures that two complementing input signals are available. Although one D-type with complementary outputs could be used, experiments showed that these two signals were not concurrent. The two outputs of the flip-flops are applied to identical RC filters. These two filters remove all the high frequency components of the pulse stream to permit further processing by conventional op-amps. The 3 dB point of these filters is set at 25 KHz; this ensures that no in-band attenuation occurs. It is important to match the components in each filter accurately. The outputs of the filters are applied to an op-amp which is configured as a differential amplifier. This ensures that the output is always the sum of a rising and falling edge of the input signal, and therefore independent of any imbalance in these edges.

The output of the operational amplifier is connected to a 600Ω resistor to produce a 600Ω unbalanced output signal which is compatible

with all the other analogue hardware. A separate 5V power supply is provided for the TTL circuits used. This ensures the maximum rejection of noise transferred down the power supplies from other logic circuits.

A3.2.2 The Summer Circuit

The modulators described in Chapter 3 produce two data outputs. To produce a single analogue output these two data outputs must be added together. The digital modulators which produce these signals weight one of them by a constant (K) so this must be compensated for before addition can take place. Calculations have shown that the weighting constant (K) must be maintained to 0.3% of its theoretical value.

The circuit of this system is shown in Figure A3.10. To relax the specification of the operational amplifiers used the scaling by K is spread over two stages. It is assumed that the two data signals have both been processed by differential output circuits, so that all the high frequency noise has been removed. The data signal which needs weighting is applied to the input of the first operational amplifier which is adjusted to attenuate by a constant factor (-P). The second data signal is applied to a similar circuit with a gain of -1. This ensures that both signals are still in phase. The scaled output is then connected to one input of the summer circuit and scaled by a constant factor, -Q, these gains are arranged so that $P \times Q = K$ thus producing the required weighting. The second data signal is applied to the second input of the summer and scaled by -1. The resulting output of the summer is then the weighted sum of the two data inputs. Some adjustment of the weighting constant is provided by the variable resistor in the feedback circuit of the first amplifier.

A3.2.3 The Filter Specifications

Three filters were used in the testing of the converters. Two of

these are identical low-pass filters and the third is a high-pass filter. All the filters are passive, with impedances of 600 Ω. The low-pass filters are seventh order elliptic with a message band of 15 KHz. Their circuit is shown in Figure A3.11a and their frequency responses plotted in Figure A3.12a. The high-pass filter is a fifth order elliptic filter with a message band of 500 Hz. Its circuit is shown in Figure A3.11b, and its corresponding frequency response is plotted in Figure A3.12b.

A3.2.4 The Ancillary Hardware

For reference, the remaining hardware, the clock generator, and a low-noise pre-amp are documented in Figure A3.13 and A3.14.

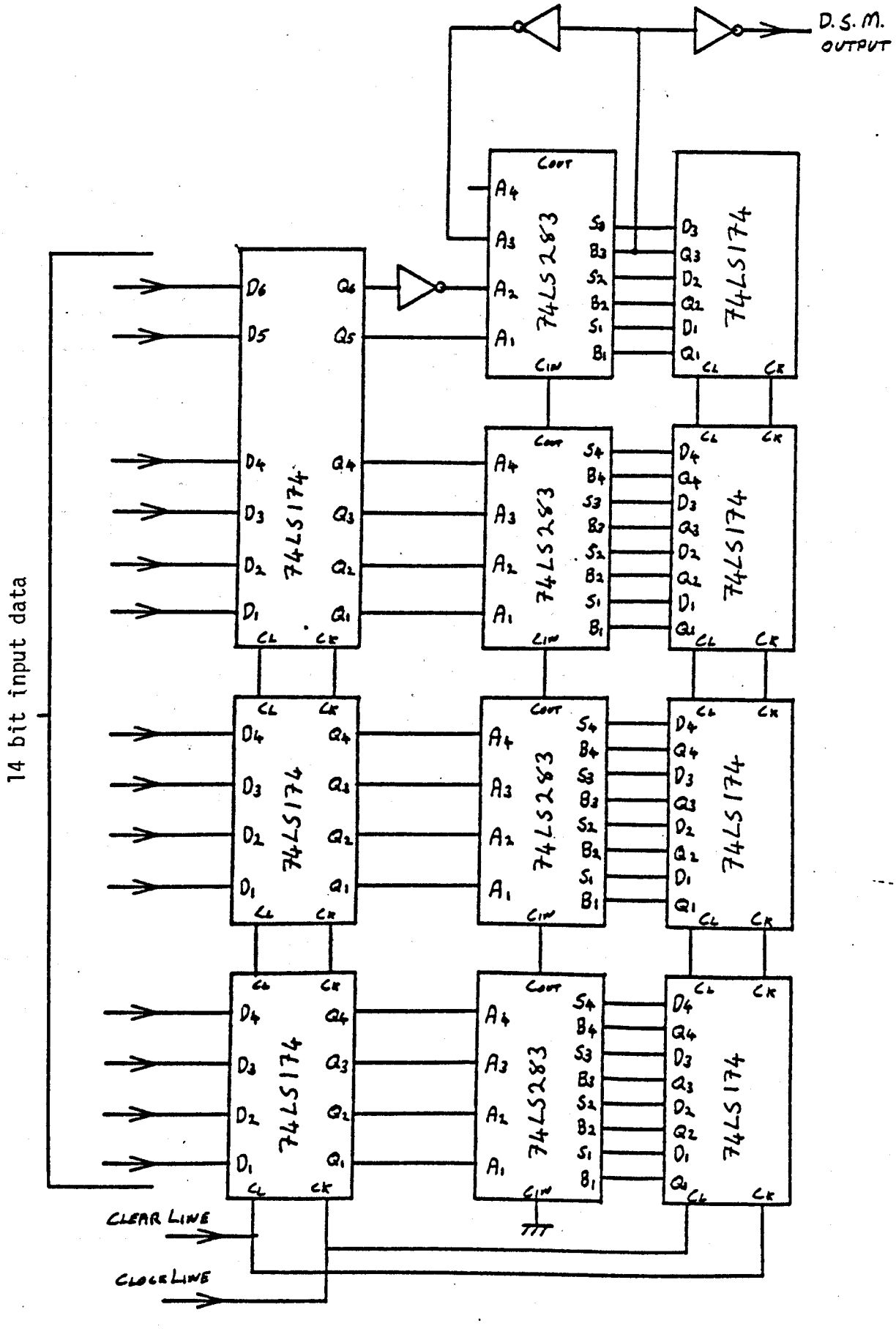


Figure A3.1 Circuit of a 14-bit d.s.m.

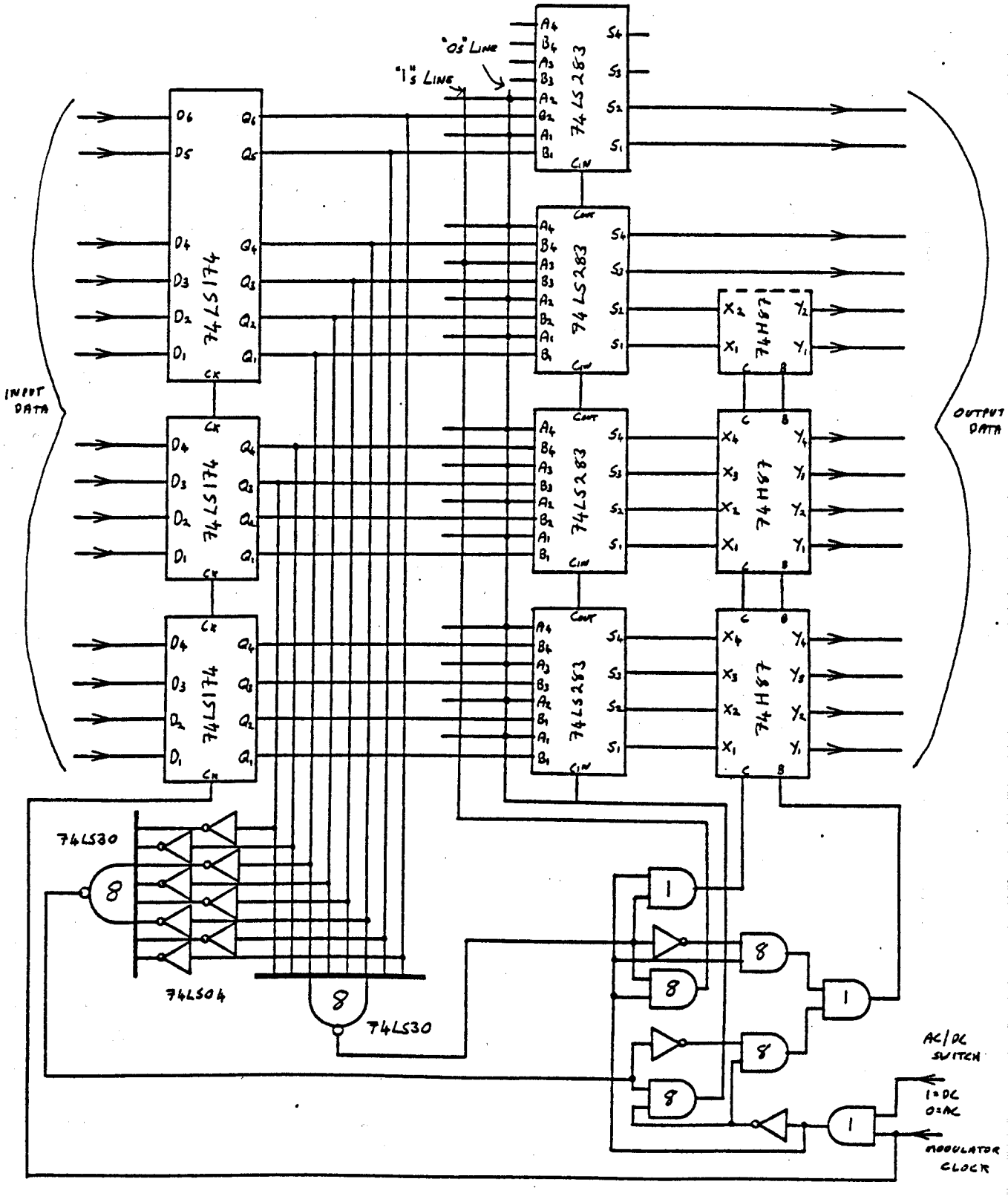


Figure A3.2 Input buffer and offset adder.

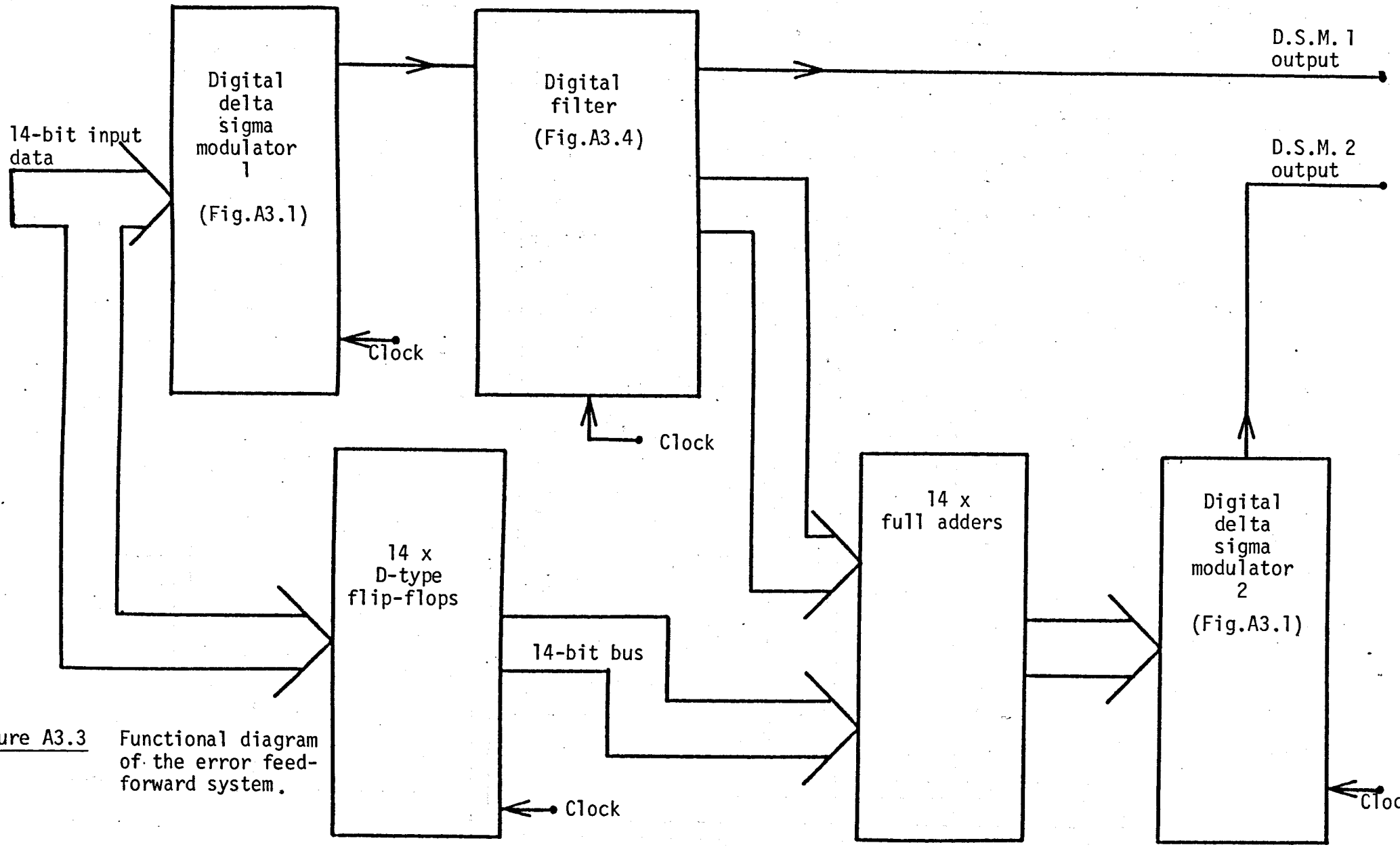


Figure A3.3 Functional diagram of the error feed-forward system.

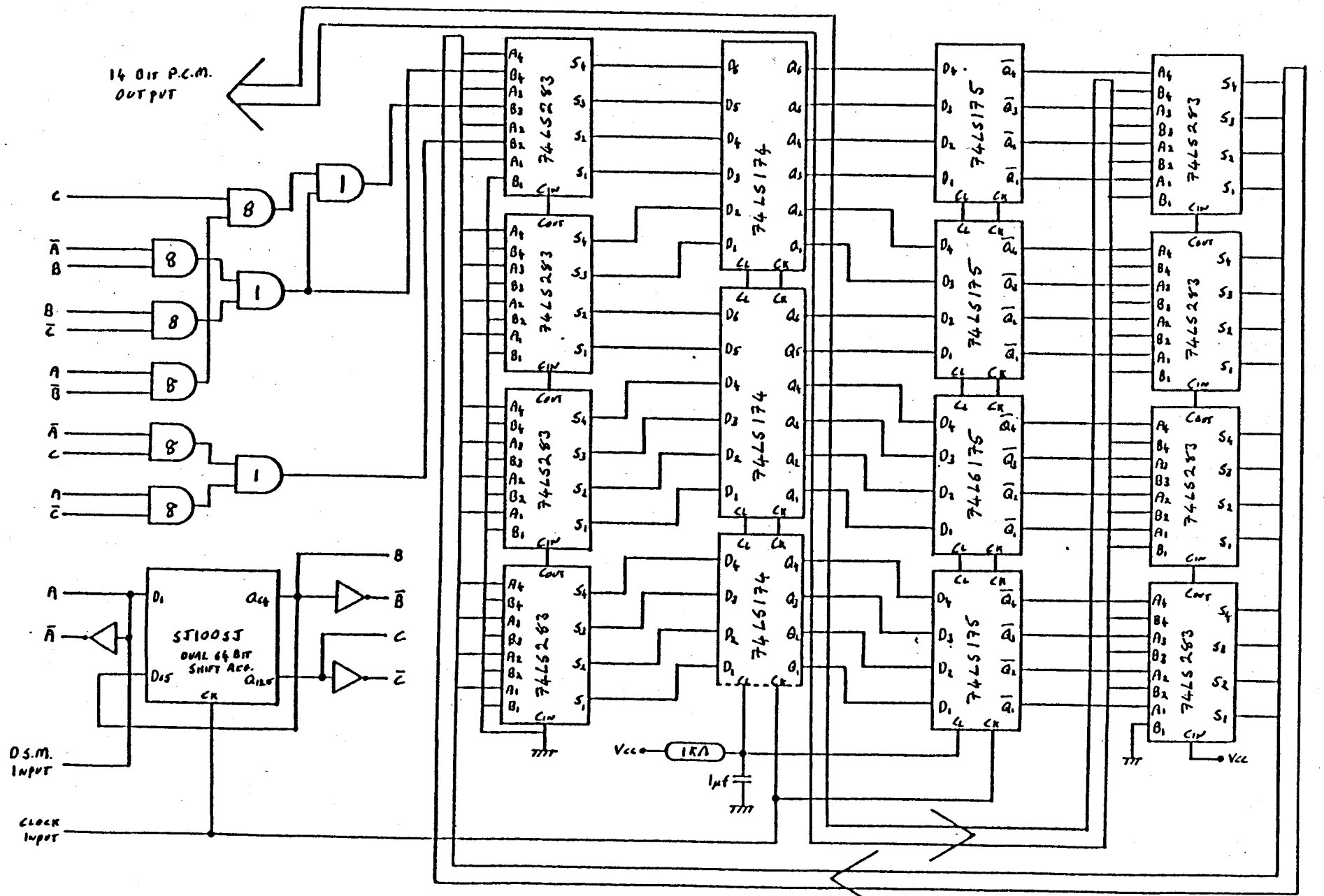


Figure A3.4 Circuit of the second order D.S.M. digital filter.

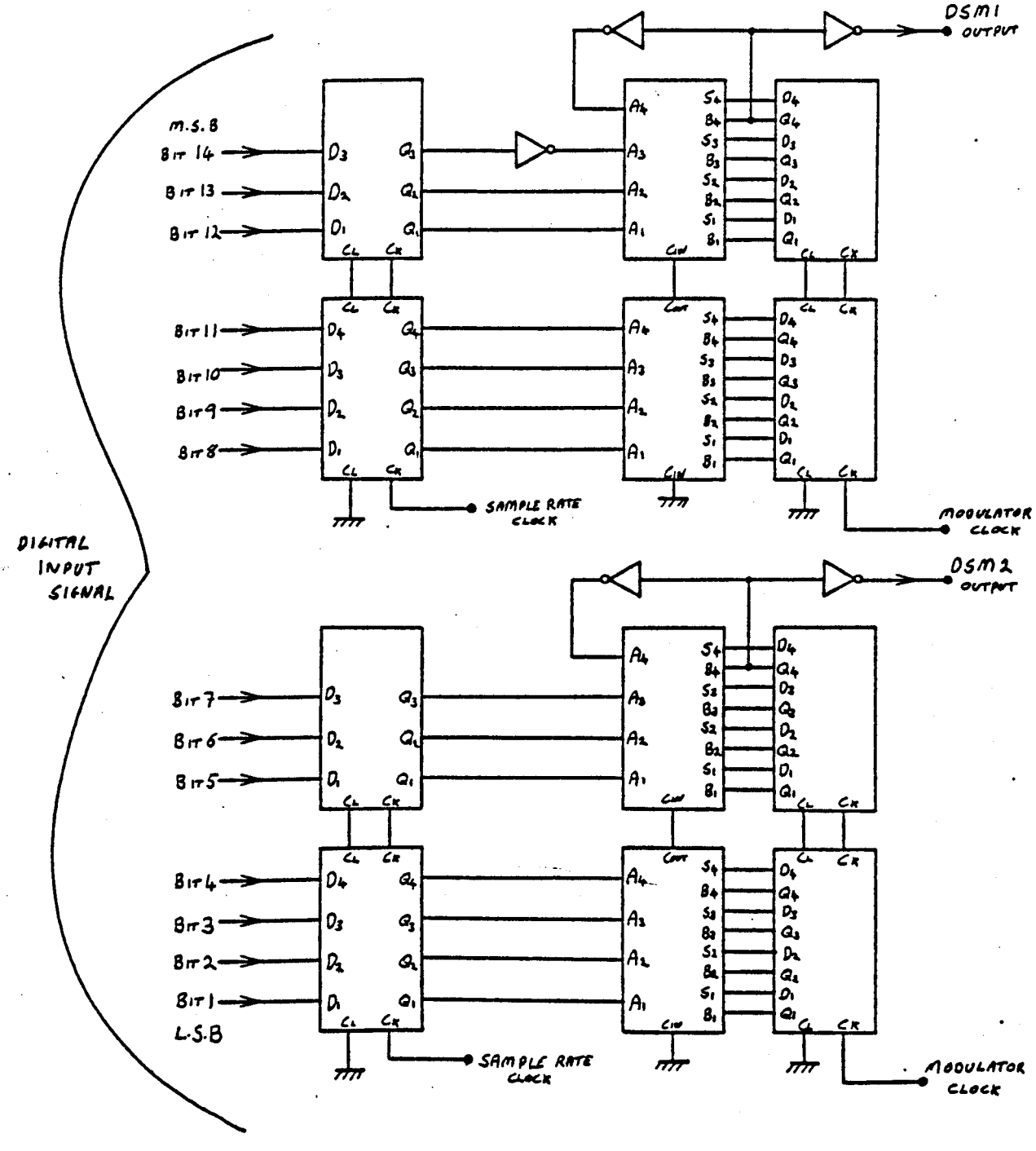
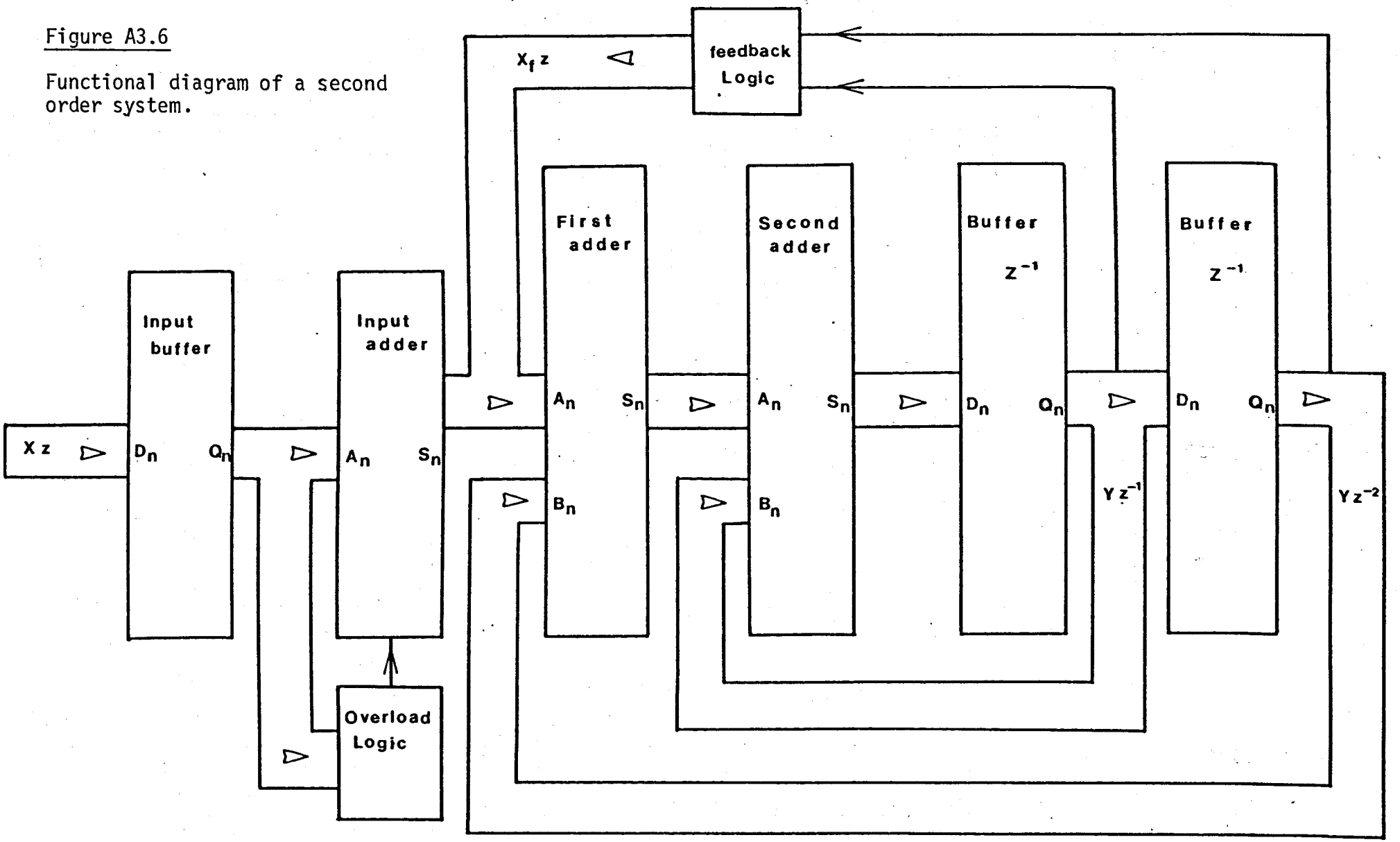


Figure A3.5 Circuit of the residual error encoder.

Figure A3.6

Functional diagram of a second order system.



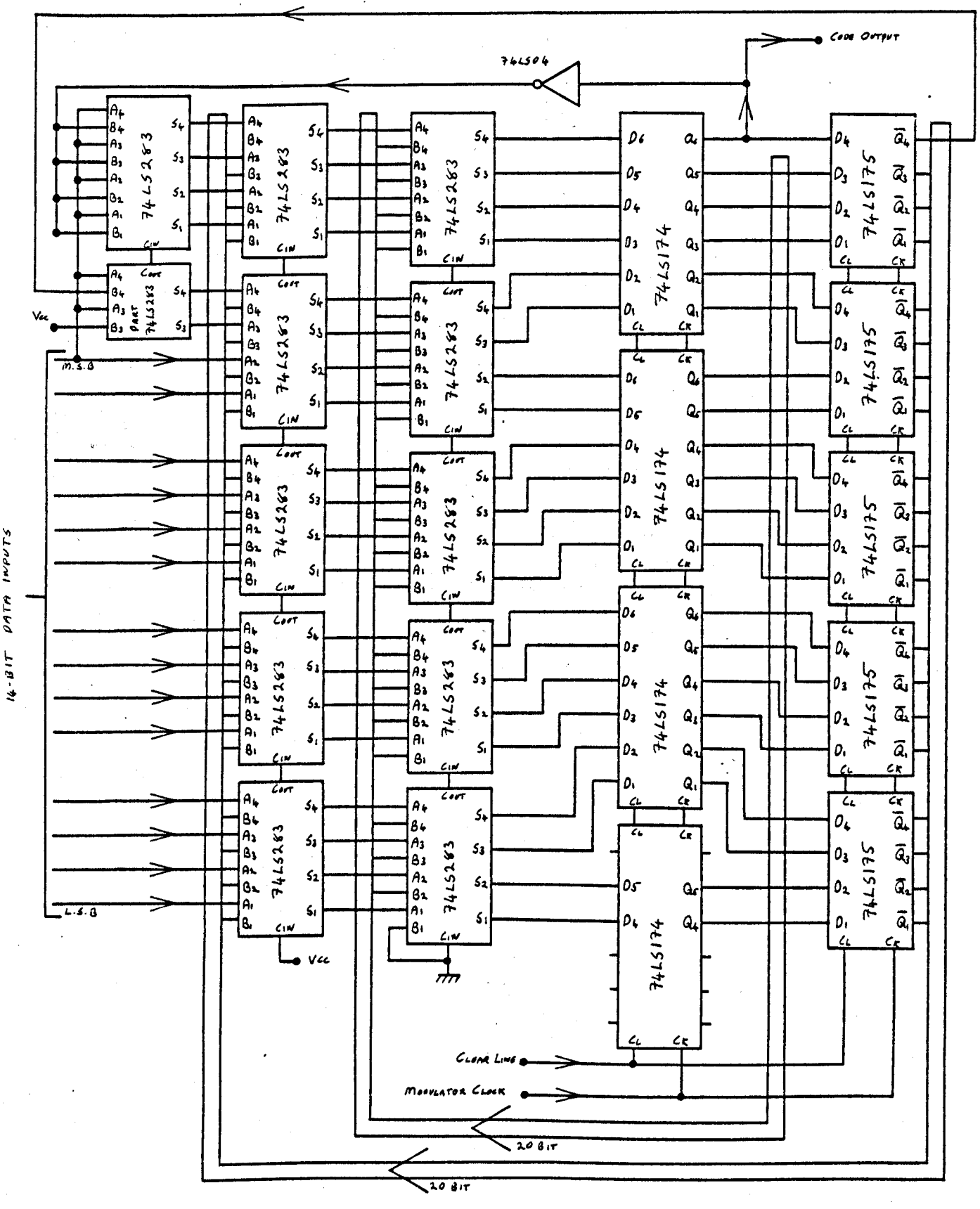


Figure A3.7 Circuit of the second order modulator.

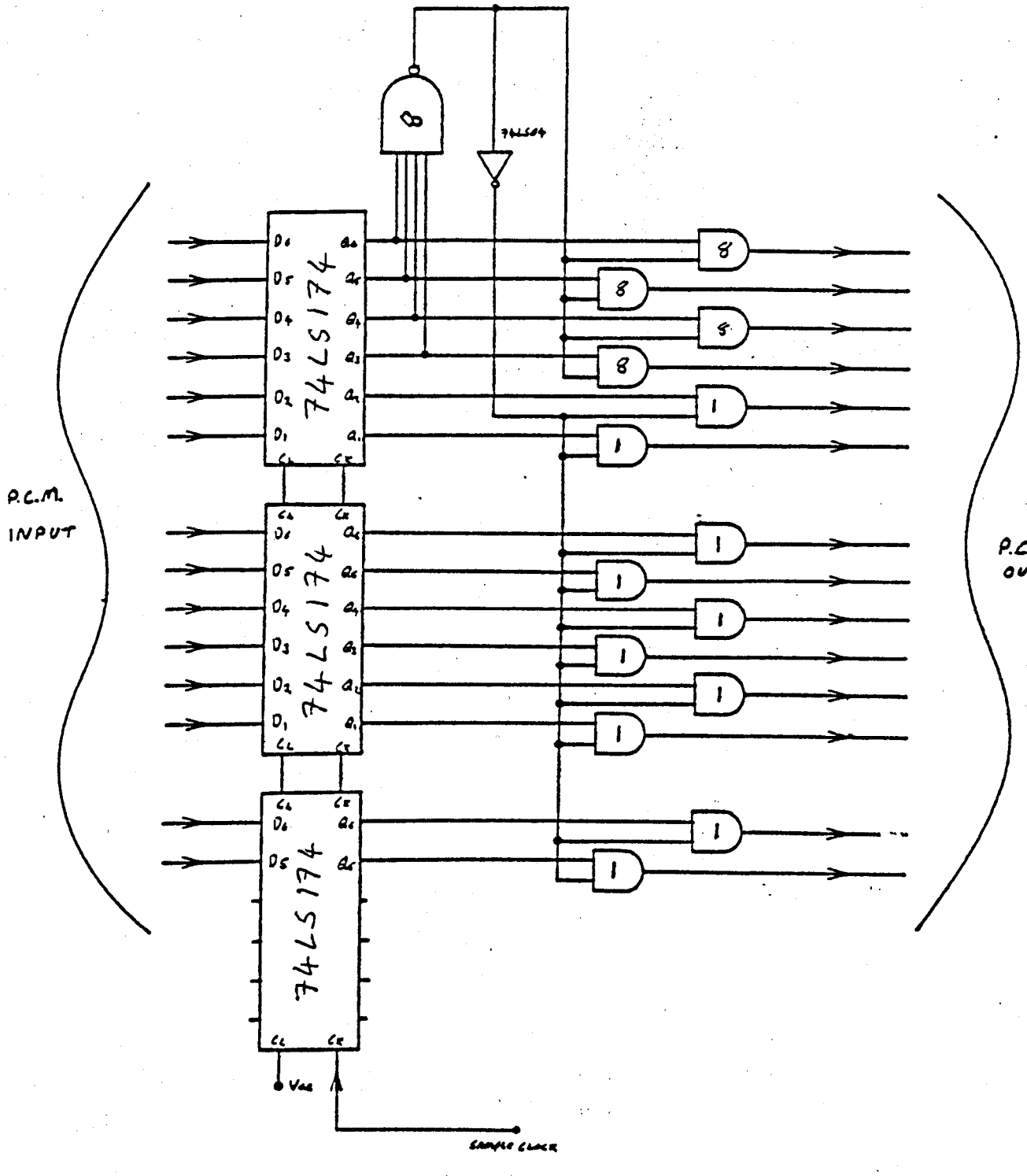


Figure A3.8 The circuit of the overload limiter.

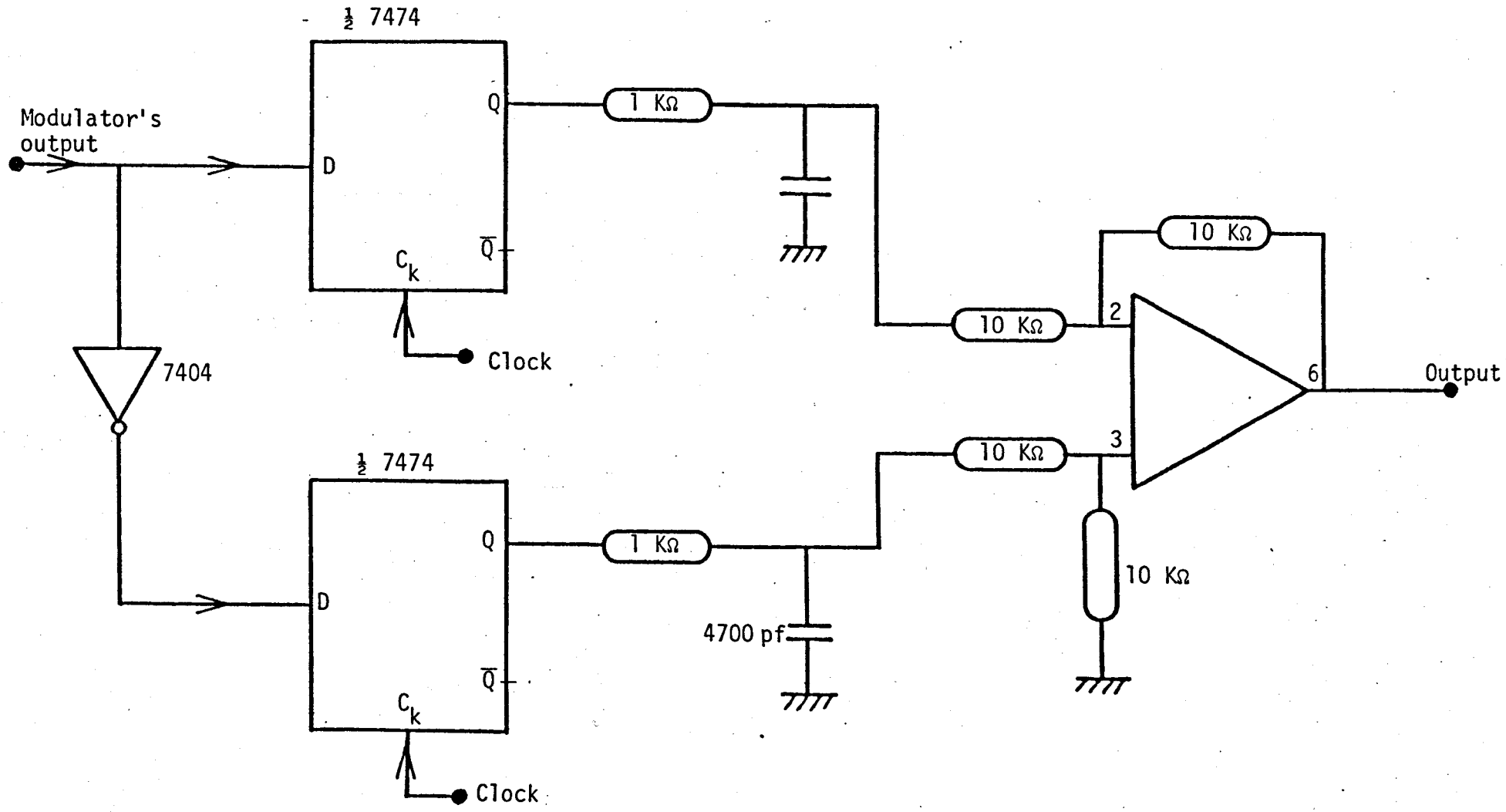


Figure A3.9 *Differential output circuit.*

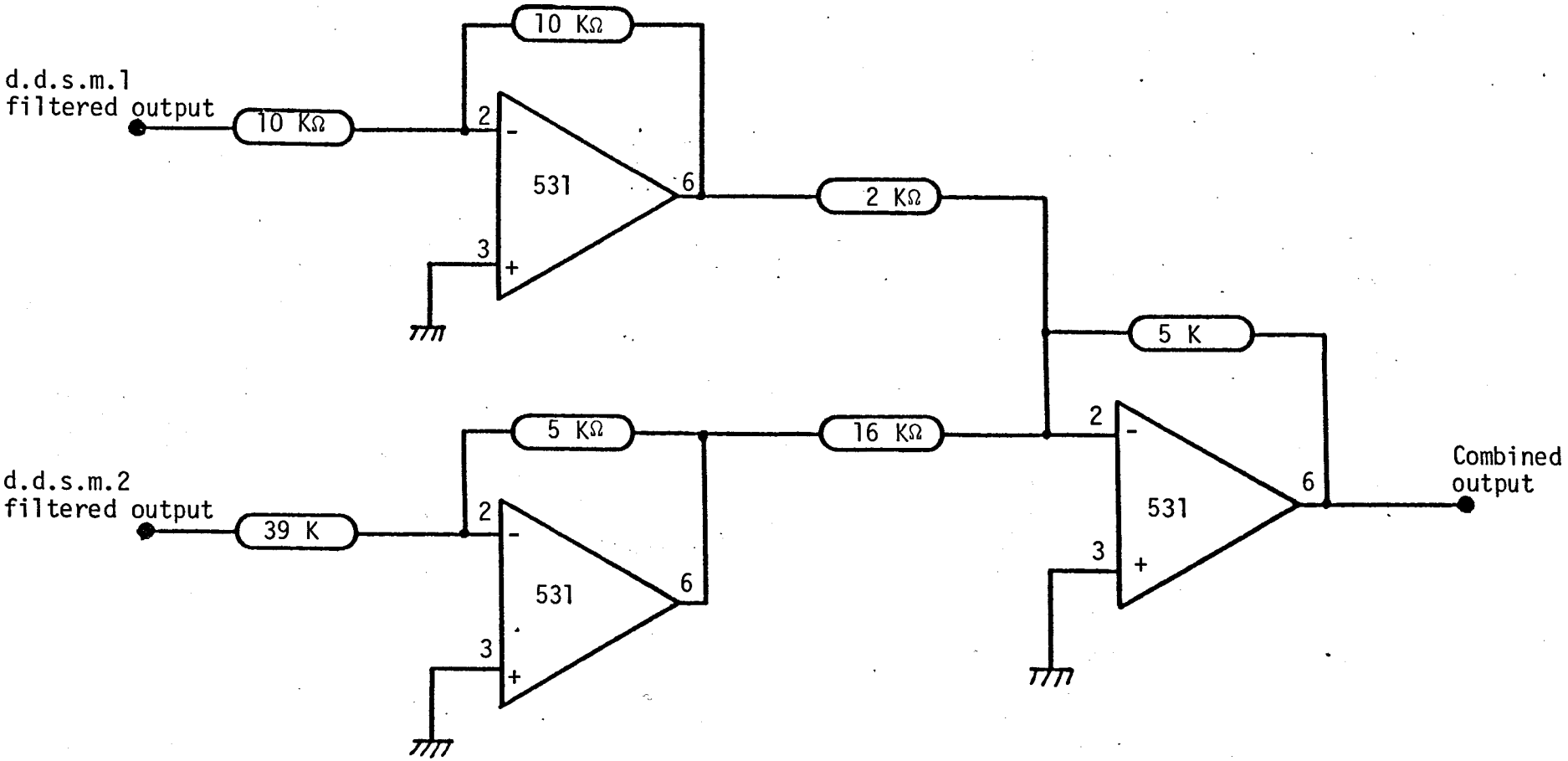
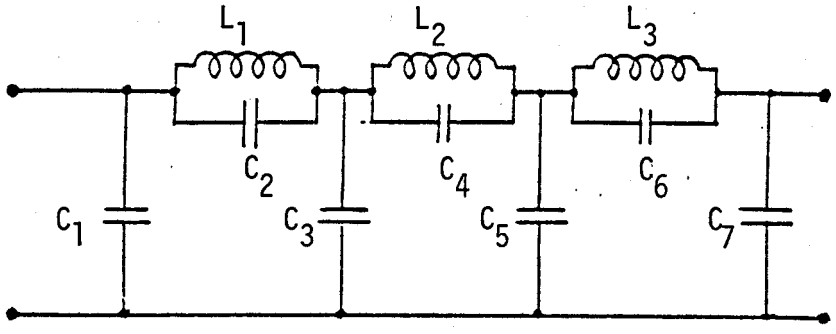


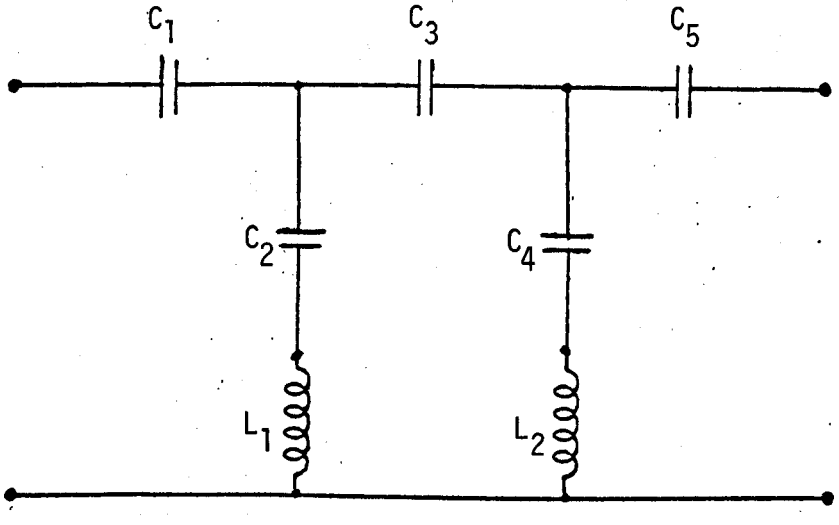
Figure A3.10 *Summer circuit for residual error encoder.*



C_1 = 0.0243 μf
C_2 = 0.00259 μf
C_3 = 0.0345 μf
C_4 = 0.00787 μf
C_5 = 0.0289 μf
C_6 = 0.0154 μf
C_7 = 0.0157 μf

L_1 = 7.63 mH
L_2 = 6.65 mH
L_3 = 4.54 mH

Figure A3.11a Circuit of the low-pass filter.



C_1 = 0.2196 μf
C_2 = 3.2625 μf
C_3 = 0.1332 μf
C_4 = 1.1925 μf
C_5 = 0.24435 μf

L_1 = 66.6 mH
L_2 = 75.15 mH

Figure A3.11b Circuit of the high-pass filter.

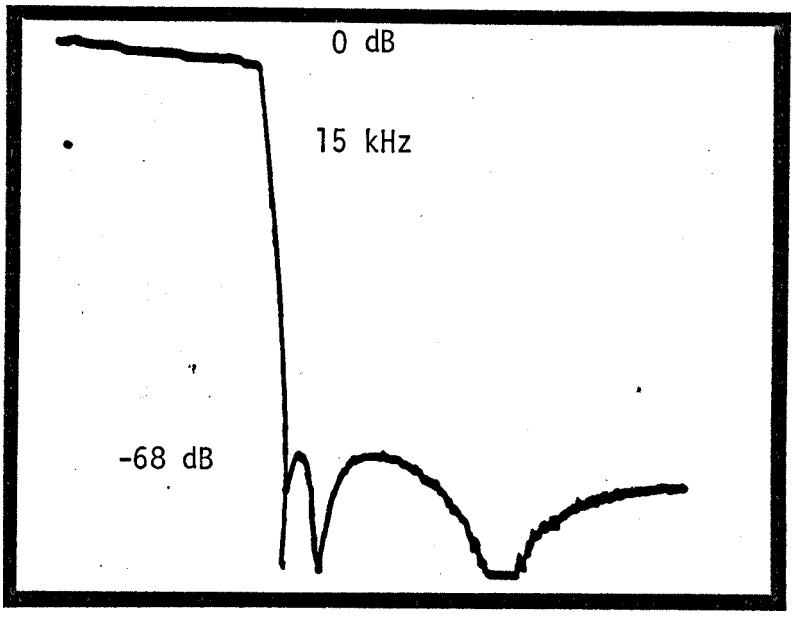


Figure A3.12a Frequency response of the low-pass filter.

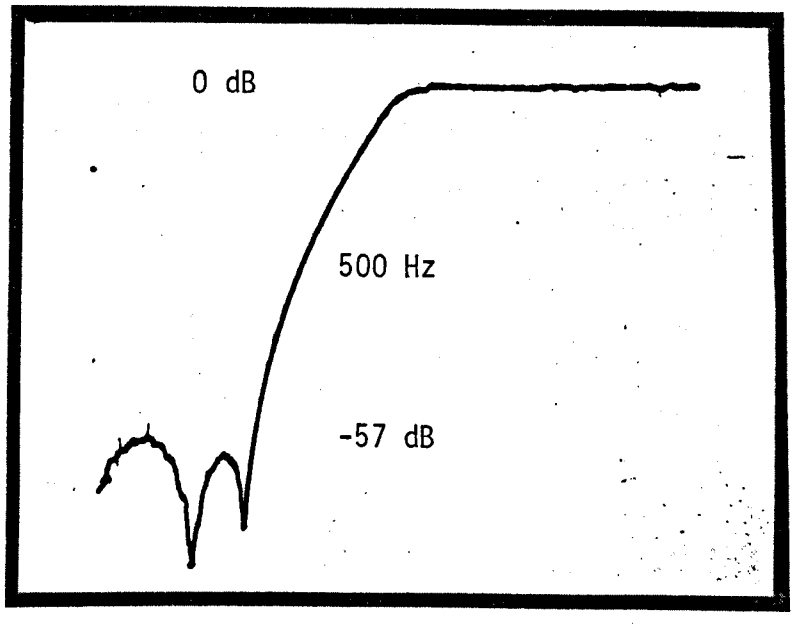


Figure A3.12b Frequency response of the high-pass filter.

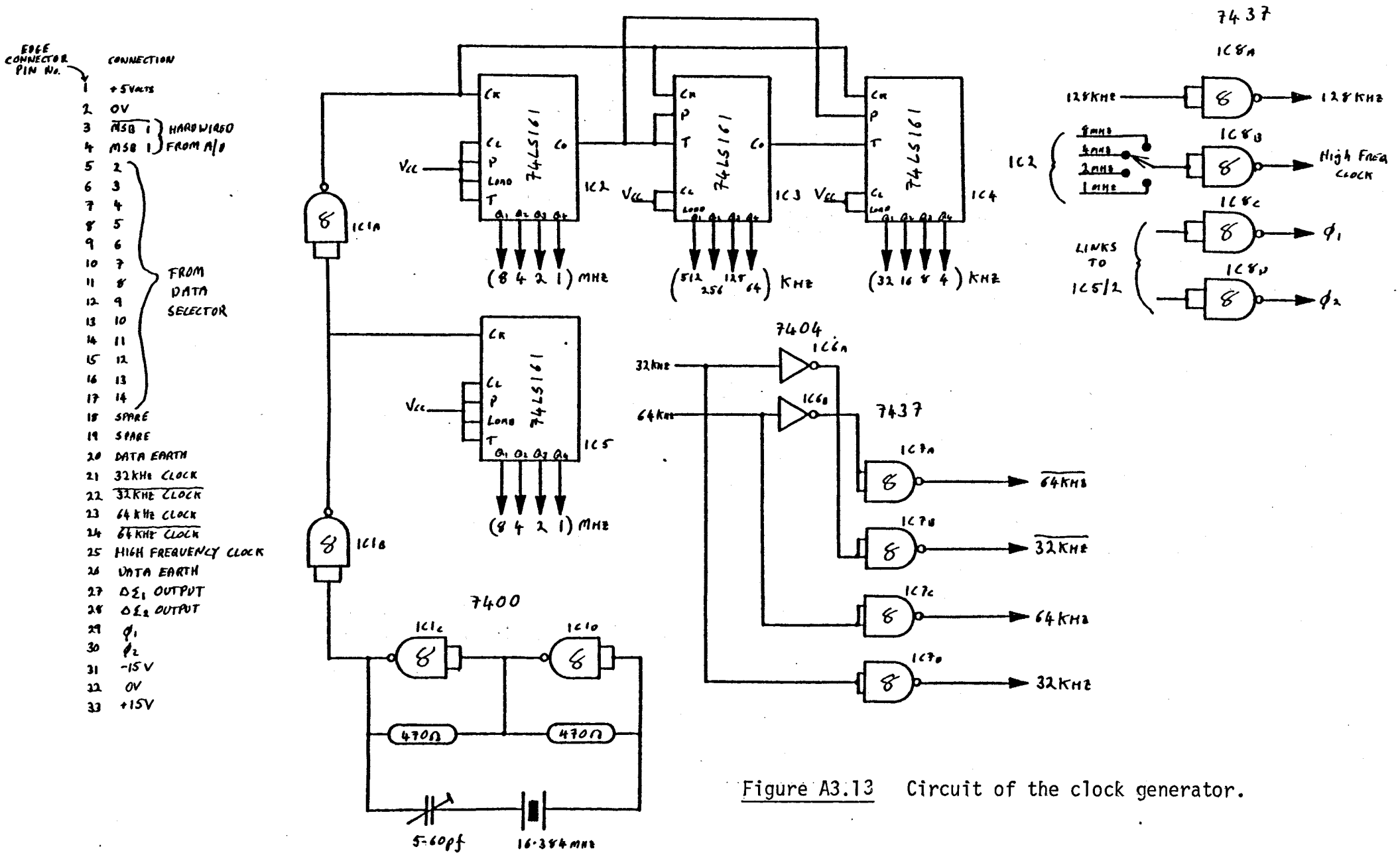


Figure A3.13 Circuit of the clock generator.

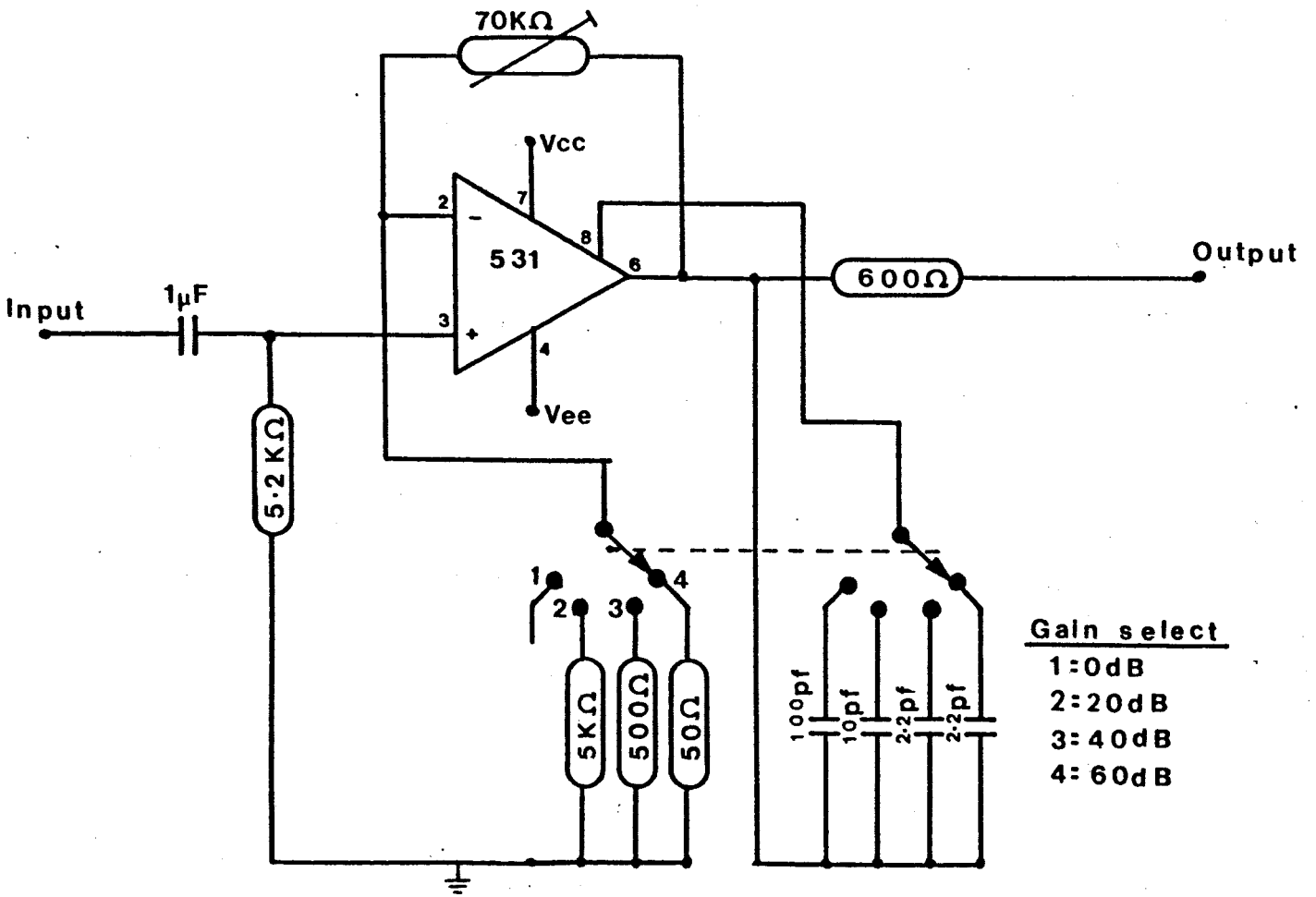
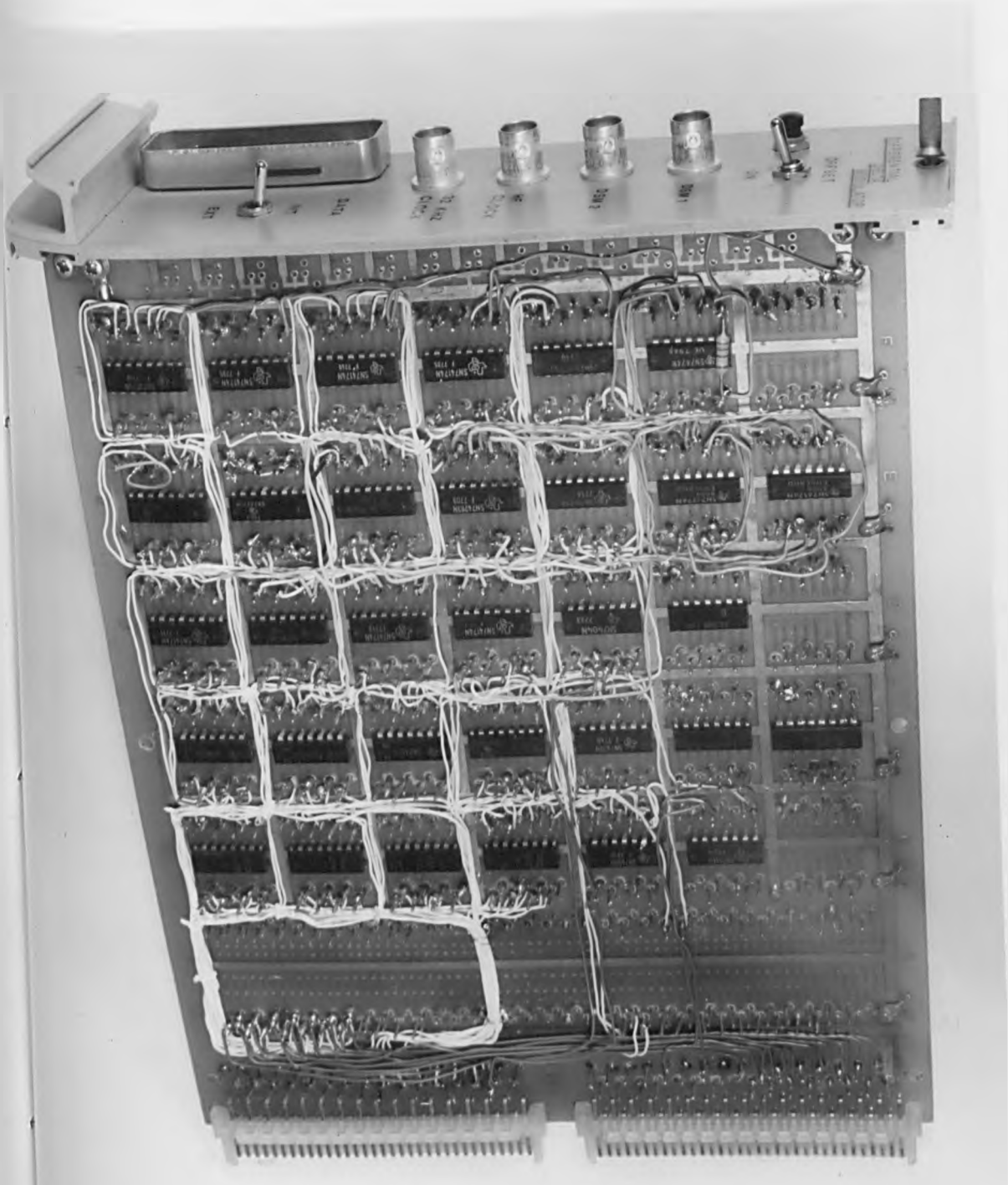
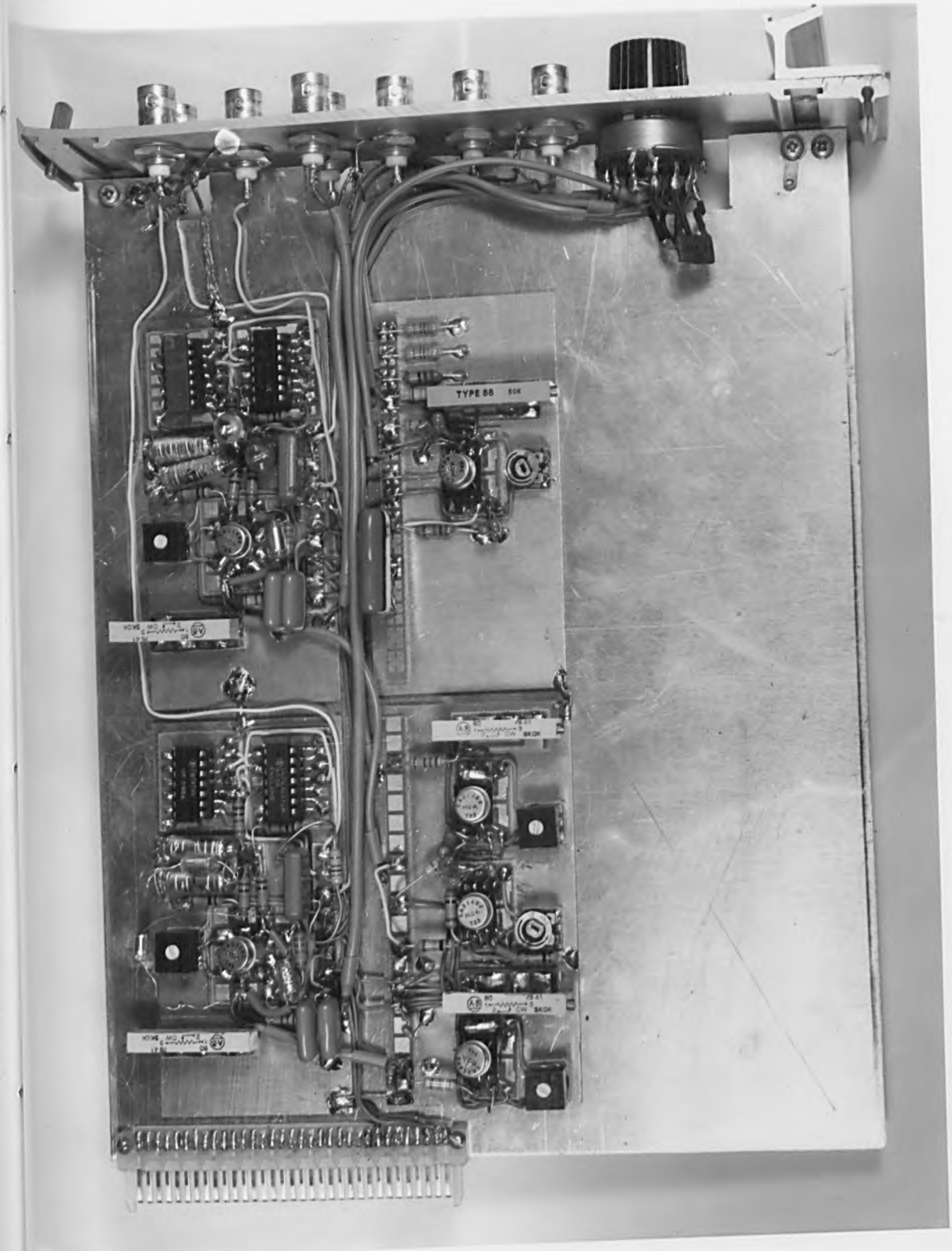


Figure A3.14 Circuit of the pre-amplifier.

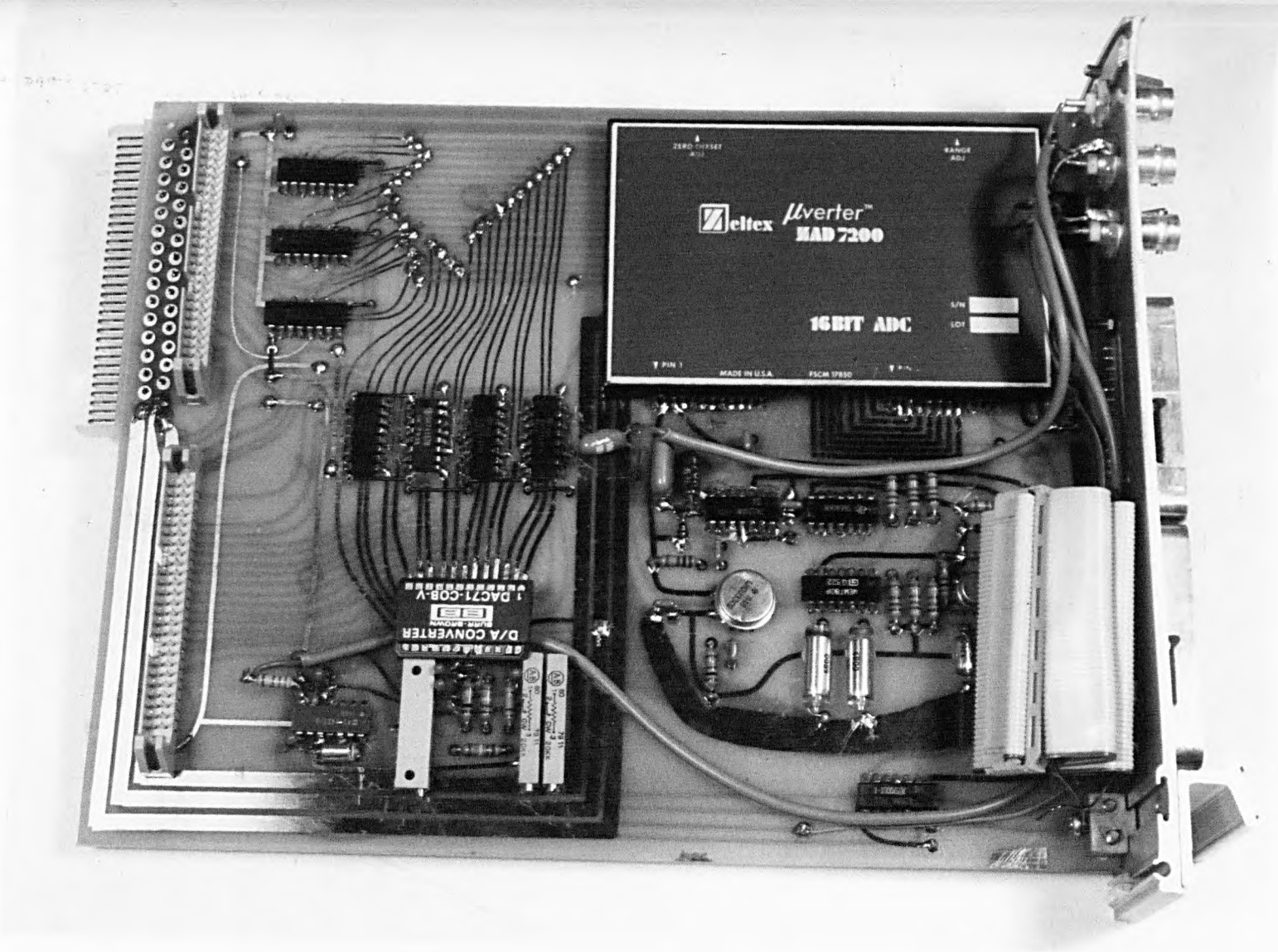
Photograph of the residual error encoder



Photograph of the analogue circuit


TYPE 88 50K

Photograph of the reference A/D - D/A


ZERO OFFSET ADJ
RANGE ADJ
Teltex μverter™
HAD 7200
16BIT ADC
S/N
LOT
PIN 1
MADE IN U.S.A.
FSCM 17850
D/A CONVERTER
DAC71-CDB-V
BURR-BROWN

APPENDIX 4

FORTRAN PROGRAM LISTINGS

A4.1 Fortran listing of program to prepare data for the microprocessor signal generator.

A4.2 Fortran listing of a typical main program used in the simulations.

A4.3 Fortran listing of subroutine DATA used to compute the sampled signals.

A4.4 Fortran listing of subroutine DSM used to simulate a first order delta sigma modulator.

A4.5 Fortran listing of subroutine SDSM used to simulate a second order system.

A4.6 Fortran listing of subroutine FFT, used to obtain the fast Fourier transform of the simulation's output data.

A4.7 Fortran listing of subroutine LAYOUT, used to format the output data.

A4.8 Fortran listing of program EDGES, used to plot the transfer characteristics of modulators with unequal rise and fall times.

A4.9 Fortran listing of program SPECTRUM which quantifies the noise introduced by the finite transitions in a modulator's output.

A4.1 Fortran listing of program to prepare data for the microprocessor signal generator

```
C     PROGRAM MAIN
C     TO TEST SUBROUTINES
C     1 DATA
C     2 PCMCON
C
C
      REAL X(512)
      WRITE(2,5)
    5 FORMAT(" ENTER THE NUMBER OF SAMPLES (MAX 512)")
      READ(1,*) NOSAMP
      CALL DATA(X,NOSAMP)
      CALL PCMCON(X,NOSAMP)
      STOP
      END
C
C
C
      SUBROUTINE DATA(X,NOSAMP)
      REAL X(NOSAMP)
      REAL PI,W,VAL
      PI=3.141593
      ITEMP=IFIX(NOSAMP)
      DO 20 II=1,ITEMP
      III=II-1
      C=FLOAT(III)
      W=(C/NOSAMP)*2.*PI
      VAL=(SIN(W)*2.**15)
      IVAL=IFIX(VAL)
      TVAL=FLOAT(IVAL)
      ERROR=VAL-TVAL
      ERROR=ABS(ERROR)
      IF(ERROR.GE.0.5)IVAL=IVAL+1
      VAL=FLOAT(IVAL)
      X(II)=VAL
   20 CONTINUE
      WRITE(6,44)
   44 FORMAT(" THE DECIMAL SAMPLES ARE ")
      WRITE(6,55)(X(J),J=1,NOSAMP)
   55 FORMAT(16(4F20.4,/))
      RETURN
      END

C
C
      SUBROUTINE PCMCON(X,NOSAMP)
      REAL X(NOSAMP),PCMVAL(512)
      INTEGER NN(4),Z(16)
      INTEGER PCM(512,16)
      DATA Z(1)/1H0/,Z(2)/1H1/,Z(3)/1H2/,Z(4)/1H3/,Z(5)/1H4/
      DATA Z(6)/1H5/,Z(7)/1H6/,Z(8)/1H7/,Z(9)/1H8/,Z(10)/1H9/
      DATA Z(11)/1HA/,Z(12)/1HB/,Z(13)/1HC/
      DATA Z(14)/1HD/,Z(15)/1HE/,Z(16)/1HF/
      BS=1.0
```

```
      WRITE(2,3)
    3 FORMAT(" INPUT NO. OF PCM BITS(INCLUDING SIGN)")
      READ(1,*)NOPCM
      DO 14 I=1,NOSAMP
      DO 114 J=1,NOPCM
  114 PCM(I,J)=0
      IF(X(I).LT.0.0)PCM(I,NOPCM)=1
      VALUE=ABS(X(I))
      ANS=0.0
  702 N=0
      IF(BS.GT.VALUE)GOTO 700
  701 N=N+1
      BV=2.**N*BS
      IF(BV.LT.VALUE)GOTO 701
      BV=2.**(N-1)*BS
      ANS=ANS+BV
      PCM(I,N)=1
      VALUE=VALUE-BV
      GOTO 702
  700 CONTINUE
      PCMVAL(I)=0.0
      NOPM=NOPCM-1
      DO 17 K=1,NOPM
      IF(PCM(I,K).EQ.1)PCMVAL(I)=PCMVAL(I)+2.**(K-1)*BS
   17 CONTINUE
      DO 51 III=1,NOPM
      IF(PCM(I,III).EQ.1)GOTO 52
   51 CONTINUE
      IF(PCM(I,NOPCM).EQ.1)PCM(I,NOPCM)=0
   52 CONTINUE
      IF(PCM(I,NOPCM).EQ.1)PCMVAL(I)=-PCMVAL(I)
      NSPARE=16-NOPCM
      DO 43 IPCM=NOPCM,1,-1
   43 PCM(I,IPCM+NSPARE)=PCM(I,IPCM)
      IF(NSPARE-1)14,45,46
   46 PCM(I,2)=0
   45 PCM(I,1)=0
   14 WRITE(6,808)(I,(PCM(I,17-J),J=1,16))
  808 FORMAT(/,I5,5X,4(4I1,3X))
      ITT=0
   39 WRITE(6,6)
    6 FORMAT(/////" HEX CONVERSION"/)
      ITT=ITT+1
      DO 64 K=1,NOSAMP
      IK=-4
      DO 55 IJ=1,4
      IK=IK+4
      J=16-IK
      NIX=PCM(K,J)*8+PCM(K,J-1)*4+PCM(K,J-2)*2+PCM(K,J-3)
   55 NN(IJ)=Z(NIX+1)
   64 WRITE(6,809)PCMVAL(K),(NN(IP),IP=1,4)
  809 FORMAT(/,F20.5,5X,4(A1,3X))
      IF(ITT.EQ.2)RETURN
      WRITE(6,337)
  337 FORMAT(//,"2'S COMPLEMENT  CONVERSION"/)
      DO 38 J=1,NOSAMP
      IF(PCM(J,16).EQ.0)GOTO 38
      DO 31 I=1,15
      GOTO(32,33) PCM(J,I)+1
```

```
 32 PCM(J,I)=1
    GOTO 31
 33 PCM(J,I)=0
 31 CONTINUE
    DO 36 I=1,16
    IF(PCM(J,I).EQ.1)GOTO 37
    PCM(J,I)=1
    GOTO 38
 37 PCM(J,I)=0
 36 CONTINUE
 38 WRITE(6,810)PCMVAL(J),(PCM(J,17-IJ),IJ=1,16)
810 FORMAT(/,F20.5,5X,4(4I1,3X))
    GOTO 39
    END
```

A4.2 Fortran listing of a typical main program used in the simulations

```
C       PROGRAM MAIN
C     THIS PROG TEST A SECOND ORDER DSM
C       SUBROUTINES:
C       1 DATA
C       2 SDSM
C       3 FFT
C      4 LAYOUT
       INTEGER OUTPUT(128,128),INPUT(128)
       INTEGER IOUT(128,128)
       INTEGER IREF(128),IDATA(33)
       REAL B(64)
       COMPLEX A(8192)
       PI=3.141593
C       IFQ SETS FREQ,OF INPUT DATA 1=500KHZ,2=1KHZ
       IFQ=1
C       IFW SETS WHERE THE FFT DATA IS NORMALIZED 1=D.C ,2=1 ST HARMONIC
       IFW=IFQ+1
       WRITE(2,98)
       READ(3,*)IPR
     2 FORMAT(5X,I4,2X,"DB ATTEN SELECTED")
       WRITE(2,3)
     3 FORMAT(5X,"ENTER INITIAL OFSET IN DSM")
       READ(3,*)L
       WRITE(IPR,4)L
     4 FORMAT(5X,I4,2X,"INITIAL VALUE OF DSM")
       WRITE(2,10)
    10 FORMAT("ENTER THE REQUIED DC OFFSET")
       READ(3,*)IOSET
       WRITE(IPR,12)IOSET
    12 FORMAT(5X,I5,"DC OFFSET")
       DO 888 IXX=1,73,6
       LL=1-IXX
       ATTEN=FLOAT(LL)/20.
       ATTEN=(10.**ATTEN)
       WRITE(IPR,2)LL
       WRITE(IPR,4)L
       WRITE(IPR,12)IOSET
       K=128
       CALL DATA(IOSET,IREF,PI,ATTEN,IFQ)
       WRITE(IPR,199)(IREF(I),I=65,128)
   199 FORMAT(8I10)
    98 FORMAT(5X,"SET OUTPUT, 2=TERMINAL, 6=LINE PRINTER")
       DO 5 I=1,64
       II=I+64
       A(I)=CMPLX(FLOAT(IREF(II)),0.0)
     5 CONTINUE
       M=6.
       N=64.
       CALL FFT(A,N,-1)
       CALL LAYOUT(A,B,POWER,33,IFW,1,IPR,1)
       POWER=ALOG10(POWER)*10.
       WRITE(IPR,999)POWER
       CALL SDSM(IREF,OUTPUT,K,L,IPR)
       K=0
       DO 30 I=65,128
```

```
      ISUM=0
      DO 20 J=1,128
      K=K+1
      ITEMP=OUTPUT(I,J)
      A(K)=CMPLX(FLOAT(ITEMP),0)
      ISUM=ISUM+ITEMP
   20 CONTINUE
      II=I-64
      INPUT(II)=ISUM
   30 CONTINUE
      CALL FFT(A,8192,-1)
      CALL LAYOUT(A,B,POWER,33,IFW,-1,IPR,2)
      POWER=ALOG10(POWER)*10.
      WRITE(IPR,999)POWER
      DO 40 I=1,64
      A(I)=CMPLX(FLOAT(INPUT(I)),0)
   40 CONTINUE
      CALL FFT(A,64,-1)
      CALL LAYOUT(A,B,POWER,33,IFW,-1,IPR,3)
      POWER=ALOG10(POWER)*10.
      WRITE(IPR,999)POWER
  999 FORMAT(//,4X,F7.3," DB=TOTAL POWER IN BAND")
  888 CONTINUE
      STOP
      END
```

A4.3 Fortran program listing of subroutine DATA used to compute the sampled signals

```
      SUBROUTINE DATA(IOSET,IREF,PI,ATTEN,IFQ)
      INTEGER INPUT(128),IERROR(128),IREF(128)
      REAL PI,VAL,W
      DO 1 I=1,128
      X=FLOAT(I)
      Y=FLOAT(IFQ)
      X=X*Y
      W=(X/64.)*2.*PI
      VAL=SIN(W)
      REF=(VAL*8191.5*ATTEN)
      ITEMP=IFIX(REF)+IOSET
      IF(ITEMP.GT.8192)ITEMP=8192
      IREF(I)=ITEMP
    1 CONTINUE
      RETURN
      END
```

A4.4 Fortran listing of subroutine DSM used to simulate a first order delta modulator

```
      SUBROUTINE DSM(INPUT,IOUT,K,L)
      INTEGER INPUT(128),IOUT(128,128),I,J,K
      IZ1=L
      DO 40 I=1,128
      IX=INPUT(I)
      DO 30 J=1,K
      IF(IZ1) 10,10,12
   10 IC1=64
      GOTO 14
   12 IC1=-64
   14 IY1=IX+IC1+IZ1
      IF(IZ1)16,16,18
   16 IOUT(I,J)=-1
      GOTO 20
   18 IOUT(I,J)=1
   20 IZ1=IY1
   30 CONTINUE
   40 CONTINUE
      RETURN
      END
```

A4.5 Fortran listing of subroutine SDSM used to simulate a second order system

```
      SUBROUTINE SDSM(INPUT,IOUT,K,L,IPR)
      INTEGER INPUT(128),IOUT(128,128),K
      IZ1=L
      IZ2=0/2
      IY1=0
      DO 40 I=1,128
      IX=INPUT(I)
      DO 30 J=1,K
      IF (IZ1) 10,10,12
   10 IC1=4*8192
      GOTO 14
   12 IC1=-4*8192
   14 IF (IZ2) 16,16,18
   16 IC2=-2*8192
      GOTO 20
   18 IC2=2*8192
   20 IY1=IX+2*IZ1-IZ2+IC1+IC2
      IF (IZ1) 22,22,24
   22 IOUT(I,J)=-1
      GOTO 26
   24 IOUT(I,J)=1
   26 IZ2=IZ1
      IZ1=IY1
      IF(IY1.GT.IMAX)IMAX=IY1
      IF(IY1.LT.IMIN)IMIN=IY1
   30 CONTINUE
   40 CONTINUE
      WRITE(IPR,50)IMAX,IMIN
   50 FORMAT("MAX NUMBER IS..",I12,"   MIN NUMBER IS...",I12)
      RETURN
      END
```

A4.6 Fortran listing of subroutine FFT used to obtain the fast fourier transform of the simulation's output data

```
      SUBROUTINE FFT(DATA, N, ISI)
      COMPLEX DATA(N)
      COMPLEX TEMP, W,CN
      IOUTD = 2
C
C CHECK FOR POWER OF TWO UP TO 15
C
      NN = 1
      DO 10 I=1,15
        M = I
        NN = NN*2
        IF (NN.EQ.N) GO TO 20
   10 CONTINUE
      WRITE (IOUTD,9999)
 9999 FORMAT (30H N NOT A POWER OF 2 FOR FOUREA)
      STOP
   20 CONTINUE
C
      PI = 4.*ATAN(1.)
      FN = N
C
C THIS SECTION PUTS DATA IN BIT-REVERSED ORDER
C
      J = 1
      DO 80 I=1,N
C
C AT THIS POINT, I AND J ARE A BIT REVERSED PAIR (EXCEPT FOR THE
C DISPLACEMENT OF +1)
C
        IF (I-J) 30, 40, 40
C
C EXCHANGE DATA(I) WITH DATA(J) IF I.LT.J.
C
   30   TEMP = DATA(J)
        DATA(J) = DATA(I)
        DATA(I) = TEMP
C
C IMPLEMENT J=J+1, BIT-REVERSED COUNTER
C
   40   M = N/2
   50   IF (J-M) 70, 70, 60
   60   J = J - M
        M = (M+1)/2
        GO TO 50
   70   J = J + M
   80 CONTINUE
C
C NOW COMPUTE THE BUTTERFLIES
C
      MMAX = 1
   90 IF (MMAX-N) 100, 130, 130
  100 ISTEP = 2*MMAX
      DO 120 M=1,MMAX
        THETA = PI*FLOAT(ISI*(M-1))/FLOAT(MMAX)
```

```
        W = CMPLX(COS(THETA),SIN(THETA))
        DO 110 I=M,N,ISTEP
          J = I + MMAX
          TEMP = W*DATA(J)
          DATA(J) = DATA(I) - TEMP
          DATA(I) = DATA(I) + TEMP
 110    CONTINUE
 120  CONTINUE
      MMAX = ISTEP
      GO TO 90
 130  IF (ISI) 160, 140, 140
C
C FOR INV TRANS -- ISI=1 -- MULTIPLY OUTPUT BY 1/N
C
  140 CN=CMPLX(FN,0)
      DO 150 I=1,N
        DATA(I) = DATA(I)/CN
 150  CONTINUE
 160  RETURN
      END
```

A4.7 Fortran program listing of subroutine LAYOUT used to format the output data

```
      SUBROUTINE LAYOUT(A,B,POWER,IR,IFW,N,IPR,IFOR)
      COMPLEX A(8192)
      REAL B(64)
      IF(IFOR-2) 12,14,16
   12 WRITE(IPR,60)
      GOTO 18
   14 WRITE(IPR,61)
      GOTO 18
   16 WRITE(IPR,62)
   18 WRITE(IPR,59)
      POWER=0
      XDB=CABS(A(IFW))
      DO 10 I=1,IR
      DBB=CABS(A(I))
      DBB=DBB/XDB
      IF(DBB.LT.0.1E-10)DBB=0.1E-10
      DB=ALOG10(DBB)*20.
      IDB=IFIX(DB)
      IF(N)3,3,2
    2 B(I)=DB
    3 IDIF=IFIX(B(I)-DB)
      WRITE(IPR,58)(I-1),A(I),IDB,IDIF
      IF(I-IFW) 4,10,4
    4 IF(I-1) 10,10,5
    5 POWER=POWER+DBB*DBB
   10 CONTINUE
   58 FORMAT(9X,I4,6X,F15.5,5X,F15.5,9X,I4,13X,I4)
   59 FORMAT(//,4X,"HARMONIC NO.",8X,"REAL PART",11X,
     ."IMAG PART",9X,"MAG. DB",9X,"DIF. DB")
   60 FORMAT(//,5X,"THE FFT OF THE 14 BIT DATA IS")
   61 FORMAT(//,5X,"THE FFT OF THE SECOND ORDER SYSTEM IS")
   62 FORMAT(//,5X,"THE FFT OF THE INTERGRATED DATA IS")
      RETURN
      END
```

A4.8 Fortran listing of program to plot the transfer characteristics of modulators with unequal rise and fall times

```
C       PROGRAM MAIN TO TEST THE EFFECT OF FINITE EDGES
C       ON THE OUTPUT OF A DSM MODULATOR
C
C
        INTEGER IOUT(128,128),INPUT(128)
        REAL DATA(128),CDATA(128),OUT(128,128)
        WRITE(2,1)
      1 FORMAT(5X,"SET OUTPUT, 2=TERMINAL, 6=LINE PRINTER")
        READ(1,*)IPR
        WRITE(2,2)
      2 FORMAT(5X,"ENTER THE INITIAL VALUE OF THE MODULATOR")
        READ(1,*)L
        WRITE(IPR,3)L
      3 FORMAT(5X,I4,2X,"INITIAL VALUE IN MOD. ")
        WRITE(2,4)
      4 FORMAT(5X,/,"SET THE RISE AND FALL TIMES (AS%)")
        READ(1,*)ITR,ITF
        TR=FLOAT(ITR)/100.
        TF=FLOAT(ITF)/100.
        WRITE(IPR,5)ITR,ITF
      5 FORMAT(/,5X,"RISE TIME SET AT",I4,"%",
     ./,5X,"FALL TIME SET AT",I4,"%")
C K SETS THE NUMBER OF LOOPS THAT ARE AVERAGED
        K=128
C I IS THE INPUT TO THE MOD.
        DO 10 I=1,128
        INPUT(I)=I-65
     10 CONTINUE
        CALL DSM(INPUT,IOUT,K,L,IPR)
C FIND THE AVERAGE AREA ON EACH MOD. LOOP
        DO 20 IROW=1,128
        IAV=0
        DO 15 ILP=1,K
        IAV=IOUT(IROW,ILP)+IAV
     15 CONTINUE
        DATA(IROW)=FLOAT(IAV)
     20 CONTINUE
C CORRECT OUTPUT DATA FOR FINITE RISE AND FALL TIME
        DO 40 JJ=1,128
        DO 35 KK=1,(K-1)
        IF(IOUT(JJ,KK).LT.IOUT(JJ,(KK+1))) GOTO 25
        IF(IOUT(JJ,KK).GT.IOUT(JJ,(KK+1))) GOTO 30
        OUT(JJ,(KK+1))=FLOAT(IOUT(JJ,(KK+1)))
        GOTO 35
     25 OUT(JJ,(KK+1))=1.-TR
        GOTO 35
     30 OUT(JJ,(KK+1))=TF
     35 CONTINUE
     40 CONTINUE
C AVERAGE CORRECTED DATA
        DO 50 IROW=1,128
        AV=0.
        DO 45 ILP=1,K
        AV=OUT(IROW,ILP)+AV
     45 CONTINUE
        CDATA(IROW)=AV
```

```
   50 CONTINUE
C  PRINT OUT DATA
      WRITE(IPR,70)
   70 FORMAT(//,5X,"COMPARISON OF INPUT DATA AND AVER. MOD. OUTPUT")
      WRITE(IPR,80)
   80
FORMAT(/,5X,"INPUT",2X,"OUTPUT",4X,"INPUT",2X,"OUTPUT",4X,"INPUT",2X
     .2X,"OUTPUT",4X,"INPUT",2X"OUTPUT")
      WRITE(IPR,100)((INPUT(II)+64),DATA(II),II=1,128)
      WRITE(IPR,85)
   85 FORMAT(//,5X,"COMPARISON OF INPUT DATA AND THE AVER. CORRECTED DAT
     .A")
      WRITE(IPR,80)
      WRITE(IPR,100)((INPUT(II)+64),CDATA(II),II=1,128)
  100 FORMAT(5X,I4,F8.1,5X,I4,F8.1,5X,I4,F8.1,5X,I4,F8.1)
      WRITE(4,110)((INPUT(II)+64),CDATA(II),II=1,128)
  110 FORMAT(I5,5X,F10.4)
      STOP
      END
C
C
C
C
      SUBROUTINE DSM(INPUT,IOUT,K,L,IPR)
      INTEGER IOUT(128,128),K,INPUT(128)
      IMAX=0
      IMIN=0
      IZ1=L
      IY1=0
      DO 40 I=1,128
      IX=INPUT(I)
      DO 30 J=1,K
      IF (IZ1) 10,10,12
   10 IC1=64
      GOTO 14
   12 IC1=-64
   14 IY1=IX+IZ1+IC1
      IF (IZ1) 16,16,18
   16 IOUT(I,J)=0
      GOTO 20
   18 IOUT(I,J)=1
   20 IZ1=IY1
      IF(IY1.GT.IMAX)IMAX=IY1
      IF(IY1.LT.IMIN)IMIN=IY1
   30 CONTINUE
CC    WRITE(IPR,60)(IOUT(I,KK),KK=1,128)
   60 FORMAT(2X,128I1)
   40 CONTINUE
      RETURN
      END
```

A4.9 Fortran listing of the program which quantifies the noise introduced by the finite transitions in a modulator's output

```
C PROGRAM TO CALCULATE THE FOURIER SERIES OF
C A DSM OUTPUT SIGNAL
C
C
      COMPLEX CRISE(32),CVD(32),CFALL(32),CHAR(32)
      INTEGER IOUT(8192),IDATA(128,128),IREF(128),IPOS(8192)
      PI=4.*ATAN(1.)
C  READ IN ALL THE USER DATA
      WRITE(2,2)
    2 FORMAT(5X,"SET OUTPUT,2=TERMINAL,6=LINE PRINTER")
      READ(3,*)IPR
      WRITE(IPR,1)
    1 FORMAT(/,5X,"RESULTS FOR A 14 BIT FIRST ORDER SYSTEM",//,)
      WRITE(2,3)
    3 FORMAT(2X,"SET. MIN,MAX,INC, FOR RISE FALL STEPS (AS % )")
      READ(3,*)IMIN,IMAX,INC
    4 FORMAT(2X,"RISE TIME",I3,"%",/,2X,"FALL TIME",I3,"%")
      WRITE(2,5)
    5 FORMAT(5X,"ENTER THE REQUIED ATTEN IN DB")
      READ(3,*) LL
      WRITE(IPR,6) LL
    6 FORMAT(5X,I4,2X,"DB ATTEN SELECTED")
      ATTEN=FLOAT(LL)/20.
      ATTEN=10.**ATTEN
C  K SETS THE CLOCK FREQ. OF THE MOD,128=4096KHZ,64=2096KHZ,ECT
      K=128
C  IFQ SETS FREQ OF DATA,1=500HZ,2=1KHZ,4=2KHZ,ECT
      IFQ=1
      CALL DATA(IREF,PI,ATTEN,IFQ)
C  L SETS THE DC OFFSET WITHIN THE MOD
      L=0
      CALL DSM(IREF,IDATA,K,L)
C  RECONFIGURE DATA INTO NEW ARAY IOUT
      IJ=0
      DO 20 I=65,128
      DO 10 J=1,K
      IJ=IJ+1
      IOUT(IJ)=IDATA(I,J)
   10 CONTINUE
   20 CONTINUE
C  CHANGE THE DATA TO LABLE THE POS. OF TRANSITIONS
C +1=RISING EDGE,-1=FALLING EDGE,0=NO CHANGE
C THE FOLLOWING THREE COUNTERS COUNT THE NUMBER OF TRANS
      IEQ=0
      IRISE=0
      IFALL=0
      DO 35 K=1,8191
      IF(IOUT(K).LT.IOUT(K+1)) GOTO 25
      IF(IOUT(K).GT.IOUT(K+1)) GOTO 30
      IPOS(K+1)=0
      IEQ=IEQ+1
      GOTO 35
   25 IPOS(K+1)=1
      IRISE=IRISE+1
      GOTO 35
   30 IPOS(K+1)=-1
```

```
      IFALL=IFALL+1
   35 CONTINUE
C  THE POS. DATA OF THE MOD OUTPUT IS IN ARAY IPOS
C  THE FOLOWING CORRECTS FOR DISCONTINUITIES AT DATA EDGES
      IF(IOUT(1).LT.IOUT(8192)) GOTO 37
      IF(IOUT(1).GT.IOUT(8192)) GOTO 38
      IPOS(1)=0
      IEQ=IEQ+1
      GOTO 39
   37 IPOS(1)=-1
      IFALL=IFALL+1
      GOTO 39
   38 IPOS(1)=1
      IRISE=IRISE+1
   39 CONTINUE
C  PRINT OUT DATA ON THE NUMBER AND TYPE OF TRANS IN DATA
      WRITE(IPR,40)IEQ,IRISE,IFALL,(IEQ+IRISE+IFALL)
   40 FORMAT(2X,"NO. OF EQUAL TRANS. IS"I5,
     ./,2X,"NO. OF RISING EDGES IS",I5,
     ./,2X,"NO. OF FALLING EDGES IS",I5,
     ./,2X,"TOTAL NO. OF TRANSITIONS IS",I5)
C START LOOP FOR DIFFERENT TR,TF
      IMIN=IMIN+1
      IMAX=IMAX+1
      DO 1000 KKK=IMIN,IMAX,INC
      ISTEP=KKK-1
      ITR=0
      ITF=ISTEP
      TR=FLOAT(ITR)/10.
      TF=FLOAT(ITF)/10.
      WRITE(IPR,4) ITR,ITF
C NOW CALCULATE THE ORG SPECTRUM FOR RISE AND FALL EDGES
      CALL ORGLIN(CRISE,CFALL,PI,TR,TF,IPR)
C  CALCULATE EACH DELAY TERM(0-N) AND MULT BY EACH
C  RISE/FALL EDGE TERM(0-N) AND ADD TO ARAT CHAR
      CALL POSPEC(CRISE,CFALL,CHAR,IPOS,PI,IPR)
 1000 CONTINUE
      STOP
      END
C
C
C
C
      REAL FUNCTION DB(A)
      B=A
      IF(B.LT.1.0E-15) B=1.0E-15
      DB=20.*ALOG10(B)
      RETURN
      END
C
C
C
C
      SUBROUTINE ORGLIN(CRISE,CFALL,PI,TR,TF,IPR)
      COMPLEX CRISE(32),CFALL(32)
      DO 10 N=1,32
      RN=FLOAT(N)
      WR=RN*PI*TR/40960.
      WF=RN*PI*TF/40960.
      VRR=(COS(WR)-1.)/(WR*RN*PI*2.)
```

```
      VFR=(1.-COS(WF))/(WF*RN*PI*2.)
      VRIT=1./(RN*2.*PI)
      VRI=VRIT-(SIN(WR)/(WR*RN*PI*2.))
      VFIT=SIN(WF)/(WF*RN*PI*2.)
      VFI=VFIT-(1./(RN*2.*PI))
      IF(WR.EQ.0.0) VRR=0.0
      IF(WR.EQ.0.0) VRI=0.0
      IF(WF.EQ.0.0) VFR=0.0
      IF(WF.EQ.0.0) VFI=0.0
      CRISE(N)=CMPLX(VRR,VRI)
      CFALL(N)=CMPLX(VFR,VFI)
   10 CONTINUE
      WRITE(IPR,20)
   20 FORMAT(//,2X,"THE ORIGINAL LINE SPECTRUM IS GIVEN FOR TESTING")
      WRITE(IPR,21)
   21 FORMAT(//,2X,"DATA FOR THE RISING EDGE")
      WRITE(IPR,22)
   22 FORMAT(/,2X,"HARMONIC NO",5X,"REAL PART",5X,"IMAG PART",5X,"MAG. (
     .DB)")
      DO 30 I=1,32
      DBR=CABS(CRISE(I))
      IDBR=IFIX(DB(DBR))
      WRITE(IPR,26)I,CRISE(I),IDBR
   26 FORMAT(2X,I7,9X,E10.4,4X,E10.4,4X,I6)
   30 CONTINUE
      WRITE(IPR,32)
   32 FORMAT(//,2X,"DATA FOR THE FALLING EDGE")
      WRITE(IPR,22)
      DO 40 I=1,32
      DBF=CABS(CFALL(I))
      IDBF=IFIX(DB(DBF))
      WRITE(IPR,26)I,CFALL(I),IDBF
   40 CONTINUE
      RETURN
      END
C
C
C
C
      SUBROUTINE POSPEC(CRISE,CFALL,CHAR,IPOS,PI,IPR)
      COMPLEX CRISE(32),CFALL(32),CHAR(32),CVD(32),CTVH
      INTEGER IPOS(8192)
      W=2.*PI/8192.
C  EMPTY THE ARAY CHAR
      DO 1 I=1,32
      CHAR(I)=CMPLX(0.0,0.0)
    1 CONTINUE
C  LOOP FOR ALL VALUES OF I
      DO 50 I=1,8192
      RI=FLOAT(I)
C  DETERMINE TYPE OF TRANS. OR JUMP IF NO TRANS.
      IVAL=IPOS(I)
      IF(IVAL.EQ.1) GOTO 10
      IF(IVAL.EQ.-1) GOTO 30
      IF(IVAL.EQ.0) GOTO 50
      WRITE(IPR,2)
    2 FORMAT(2X,"POS. ERROR IN ARAY,TRAP SUBROUTINE POSPEC")
C  RISING EDGES
C  CALCULATE THE DELAY TERM FOR VALUE OF I FOR ALL VALUES OF N
   10 DO 12 N=1,32
```

```
      RN=FLOAT(N)
      VDR=COS(W*RN*RI)
      VDI=SIN(W*RN*RI)
      CVD(N)=CMPLX(VDR,VDI)
   12 CONTINUE
C  MULT ARAY CRISE BY DELAY ARAY CVD ADD TO ARAY CHAR
      DO 15 N=1,32
      CTVH=CRISE(N)*CVD(N)
      CHAR(N)=CHAR(N)+CTVH
   15 CONTINUE
      GOTO 50
C  FALLING EDGES
C  CALCULATE THE DELAY TERM FOR VALUE OF I FOR ALL VALUES OF N
   30 DO 32 N=1,32
      RN=FLOAT(N)
      VDR=COS(W*RN*RI)
      VDI=SIN(W*RN*RI)
      CVD(N)=CMPLX(VDR,VDI)
   32 CONTINUE
C  MULT ARAY CFALL BY DELAY ARAY CVD ADD TO ARAY CHAR
      DO 35 N=1,32
      CTVH=CFALL(N)*CVD(N)
      CHAR(N)=CHAR(N)+CTVH
   35 CONTINUE
   50 CONTINUE
C  PRINT OUT ARAY CHAR
      WRITE(IPR,60)
   60 FORMAT(/,2X,"DATA FOR THE SUM OF ALL HARMONIC LEVELS")
      WRITE(IPR,61)
   61 FORMAT(/,2X,"HARMONIC NO",5X,"REAL PART",5X,"IMAG PART",5X,"MAG. (
     .DB)")
   62 FORMAT(2X,I7,9X,E10.4,4X,E10.4,4X,F9.4)
      TEMP=0.
      DO 70 I=1,32
      VHAR=CABS(CHAR(I))
      TEMP=TEMP+VHAR*VHAR
      HARDB=DB(VHAR)
      WRITE(IPR,62)I,CHAR(I),HARDB
   70 CONTINUE
      POWDB=DB(TEMP)/2.
      WRITE(IPR,75) POWDB
   75 FORMAT(//,5X,"TOTAL POWER IS",F10.5,//)
      RETURN
      END
C
C
C
C
      SUBROUTINE DATA(IREF,PI,ATTEN,IFQ)
      INTEGER IREF(128)
      REAL PI,VAL,W
      DO 1 I=1,128
      X=FLOAT(I)
      Y=FLOAT(IFQ)
      X=X*Y
      W=(X/64.)*2.*PI
      VAL=SIN(W)
      REF=(VAL*8192.*ATTEN)
      IREF(I)=IFIX(REF)
    1 CONTINUE
```

```
      RETURN
      END
C
C
C
C
      SUBROUTINE DSM(INPUT,IOUT,K,L)
      INTEGER INPUT(128),IOUT(128,128),I,J,K
      IZ1=L
      DO 40 I=1,128
      IX=INPUT(I)
      DO 30 J=1,K
      IF(IZ1) 10,10,12
   10 IC1=8192
      GOTO 14
   12 IC1=-8192
   14 IY1=IX+IC1+IZ1
      IF(IZ1)16,16,18
   16 IOUT(I,J)=0
      GOTO 20
   18 IOUT(I,J)=1
   20 IZ1=IY1
   30 CONTINUE
   40 CONTINUE
      RETURN
      END
```