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Memristive effects due to charge transfer in graphene gated through ferroelectric $CuInP_2S_6$

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Keywords: van der Waals Ferroelectrics, two-dimensional materials, electrical transport, $CuInP_2S_6$, Graphene

Abstract

Ferroelectricity at the nanometre scale can drive the miniaturisation and wide application of ferroelectric devices for memory and sensing applications. The two-dimensional van der Waals (2D-vdW) ferroelectrics $CuInP_2S_6$ (CIPS) has attracted much attention due to its robust ferroelectricity found in thin layers at room temperature. Also, unlike many 2D ferroelectrics, CIPS is a wide band gap semiconductor, well suited for use as a gate in field-effect transistors (FETs). Here, we report on a hybrid FET in which the graphene conducting channel is gated through a CIPS layer. We reveal hysteresis effects in the transfer characteristics of the FET, which are sensitive to the gate voltage, temperature and light illumination. We demonstrate charge transfer at the CIPS/graphene interface in the dark and under light illumination. In particular, light induces a photodoping effect in graphene that varies from *n*- to *p*-type with increasing temperature. These hybrid FETs open up opportunities for electrically and optically controlled memristive devices.

1. **Introduction**

Since the discovery of graphene [1], two-dimensional (2D) van der Waals (vdW) materials have attracted much interest due to their unique electrical [2], magnetic [3], thermal

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[4] and optical properties [5-6]. In particular, the formation of hybrid heterostructures and functional interfaces offer exciting opportunities for a wide range of multifunctional devices [3-5]. Amongst materials of interest, ferroelectrics based on 2D layered vdW crystals have received much attention due to their stable and switchable spontaneous polarization (**P**) in atomically thin layers and up to room temperature [7,8]. Thus, they are ideally suited for device miniaturization that is difficult to achieve by conventional ferroelectrics due to intrinsic size-related effects [9,10]. Examples of vdW ferroelectrics include In_2Se_3 [11-16], $CuInP_2S_6$ (CIPS) [17-21], SnTe [22], WTe_2 [23], *etc*. Their combination with graphene could facilitate the integration of their rich electronic and optical properties with graphene-based nanoelectronics [24].

Within the family of vdW ferroelectrics, CIPS is of particular interest due to its relatively high Curie temperature (T_c = 315 K) and out-of-plane ferroelectricity [17-20, 25-29]. This compound belongs to a class of transition metal thio/selenophosphates (TPS) in which the metal cations (In^{3+} and Cu^{1+}) are embedded in the lattice framework of thiophosphate $(P_2S_6)^{4-}$ or selenophosphate $(P_2Se_6)^{4-}$. Each vdW layer consists of a close-packed framework of S-atoms in which the Cu^{1+}, In^{3+} and the P-P pairs fill the octahedral voids [27, 30, 31]. In the ferroelectric phase, Cu^{1+} shift upward or downward relative to the midplane of each vdW layer, leading to an out-of-plane polarization **P**, which is stable down to bilayers [18]. Thus, CIPS can be used in combination with other 2D materials to realize ferroelectric field effect transistors (FeFET) [23, 32-36], negative capacitance transistors [37, 38], photodetectors [39], ferroelectric tunnel junctions (FTJs) [20, 40], memristors [41] and devices for energy applications [42-43]. In particular, since the electrostatic potential at the graphene/ferroelectric interface can be modified by switching the ferroelectric polarization [20, 40, 44], devices combining heterostructural CIPS and graphene are of particular interest. These could offer a route to low power electronics and non-volatile switching for memory and computing applications. Also, compared to conventional ferroelectrics [45-54], the semiconducting properties of CIPS could

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offer possibilities for the optical manipulation of electrical properties. Despite these prospects, the mechanisms associated with the resistive switching behaviour of CIPS-based devices remain poorly understood. Systematic studies of CIPS under different conditions (*e.g.* temperature, electric fields, light) can help to unravel the complex interplay between various hysteric effects caused by ferroelectricity, ionic conductivity, crystal defects, *etc*. [55]. These are required to develop effective strategies for future applications.

Here, we use graphene as a sensitive probe of polarization and charge transfer phenomena at the CIPS/graphene interface. For this purpose, we use hybrid FETs in which the graphene conducting channel is gated through a CIPS layer (Figure 1a,b). The transfer characteristics of these FETs reveal hysteretic and memristive effects, which are sensitive to gating, temperature and light illumination. A range of functionalities are observed in these devices, including photoresponsivity by photodoping of graphene induced by CIPS. The underlying mechanisms of conduction are examined over a range of temperatures and under light excitation to account for different resistive switching mechanisms.

2. Results and discussion

2.1 Room temperature memristive effects in CIPS/graphene FETs

The CIPS/graphene heterostructures were assembled by exfoliation and mechanical stamping of individual graphene and CIPS flakes inside a glovebox (see Experimental Section). Figure 1a shows the optical image of a CIPS/graphene multi-terminal FET on a SiO_2/*n*-Si substrate. The CIPS flake lies under one section of the graphene layer. The two sections of the device comprising pristine graphene (PG) and the CIPS/graphene heterostructure (CG) are in a series resistance configuration with the same electrical current, I, flowing through both of them. Thus, by monitoring the voltage drop, V, across different pairs of terminals along the graphene channel, we can study simultaneously the conductive properties of PG and CG (Figure 1a). The I-V curves of the PG and CG layers are ohmic. The corresponding longitudinal resistance, R, was measured over a range of gate voltages V_G applied between the graphene and the Si-gate

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electrode (Figure 1b). Electrical transport experiments were conducted in darkness and with the device uniformly illuminated by an unfocused laser beam of photon energy $h\nu$ = 3.06 eV (λ = 405 nm) larger than the band gap energy of bulk CIPS (E_g = 2.7 eV at T = 300K) [59].

Details of the fabrication and preliminary characterisation of the CIPS flakes are in the experimental section and Figure S1 and S2 of the Supplementary Information S1. Figure 1c shows the typical Raman spectrum for bulk CIPS at T = 300K. It shows peaks due to the vibrational modes of $P_2S_6^{4-}$ (102 cm^{-1}, 115 cm^{-1}), S-P-S (215 cm^{-1}, 242 cm^{-1}, 267 cm^{-1}), Cu^{1+}/In^{3+} (317cm^{-1}), P-P (375 cm^{-1}), P-S (450 cm^{-1}) and S-P-P (162 cm^{-1}), as reported for the ferroelectric phase of CIPS [29, 33]. Similar Raman spectra were observed in nanometer-thick layers (Figure S1 in the Supplementary Information S1).

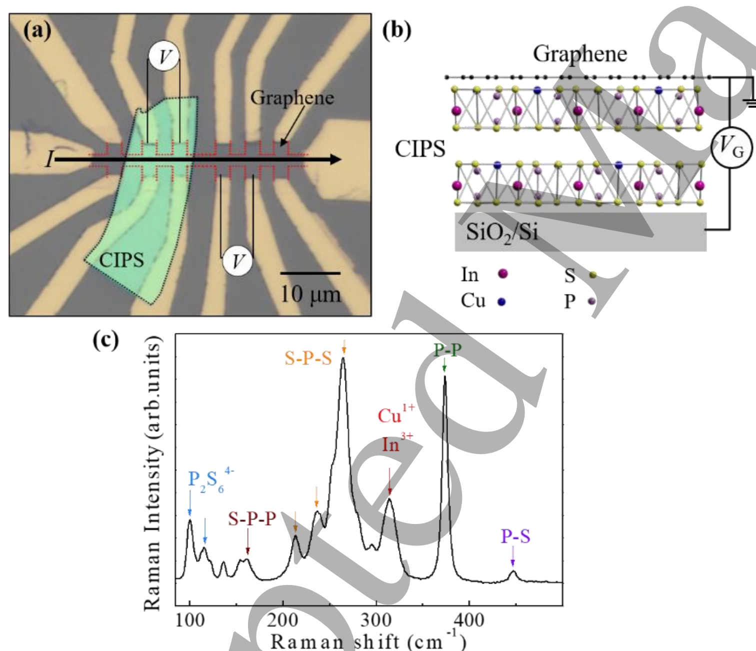

Figure 1: CIPS/graphene heterostructures. (a) Optical image of a CIPS/graphene multi-terminal field effect transistor on a SiO_2/n-Si substrate. Red and black dashed lines mark the edges of the graphene and CIPS layers, respectively. The thickness of the CIPS flake is t = 50 nm. (b) Schematic of the CIPS/graphene heterostructure and crystal structure of graphene and CIPS. The gate voltage V_G is applied between the graphene and the Si-gate electrode. (c) Raman spectrum of bulk CIPS showing peaks due to different vibrational modes (T = 300 K, P = 200 µW, λ = 532 nm).

For pristine graphene grown by CVD (chemical vapour deposition), the longitudinal resistance, R, has a maximum at around a gate voltage V_G = 5 V corresponding to the charge neutrality point V_{NP} of the graphene Dirac cone (see dashed lines in Figure 2a and Figure S3a in the Supplementary Information). Thus, our pristine graphene layers are p-type doped. We

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estimate a hole density $p = 3.2x10^{11}$ cm^{-2} at $V_G = 0$. The electron and hole mobilities are $\mu = 4.6\times10^3$ cm^2/Vs and 4.2×10^3 cm^2/Vs at $T = 300$ K, respectively. This slight asymmetry in electron and hole mobility is due to the attractive versus repulsive scattering of carriers by charged impurities in the substrate and/or on the surface of graphene due to unintentional doping of CVD graphene [61,62]. All PG samples reveal a small hysteresis ($\Delta V_{NP} < 4$ V) in the transfer curve (Figure 2a and Figure S3b-c in the Supplementary Information). Furthermore, the R (V_G) curves do not change significantly when graphene is illuminated with laser light (Figure S3d). As discussed below, these properties are modified in the CG FET.

Figure 2a shows the R (V_G) curve for the CG section of the FET. The curve is shifted to lower V_G compared to PG. The shift is accompanied by a shift in the graphene charge neutrality point ($\Delta V_{NP} = 9$ V) for a gate voltage sweep of $\Delta V_G = \pm 20$ V. For the R (V_G) curve in Figure 2a, the transfer curve is acquired starting from $V_G = 0$ (mark 1 in Figure 2a), continuing with a sweep of V_G to a maximum $V_G = + 20$ V (mark 2), passing through $V_G = 0$ V again along the way down (mark 3) to a minimum $V_G = - 20$ V (mark 4). As shown in Figure 2b, the temporal response of the resistance at $V_G = 0$ V is slow (with rise and decay times of $\tau > 100$ s) and different following a sweep down or a sweep up of V_G. Thus, our data indicate that CIPS modulates the carrier density of the graphene layer, inducing an n-type doping at $T = 300$ K. To date, both p-type or n-type doping of graphene and hysteretic behaviours have been reported in different FE/graphene heterostructures [46, 50-51, 53-54, 56-57]. Here, we examine the nature of the doping and hysteresis in the CIPS/graphene heterostructure by considering the dependence of the hysteresis on the gate voltage, the time scale at which this takes place, and its dependence on temperature and light illumination.

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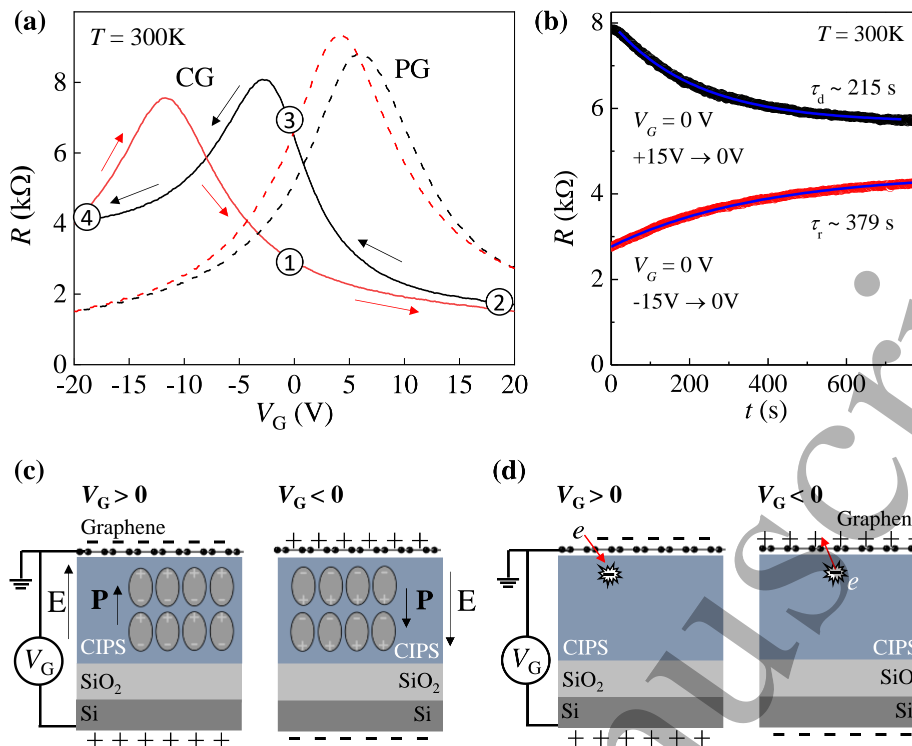

Figure 2: Room temperature transfer curves of field effect transistors based on CIPS/graphene (CG). (a) Transfer curves $R(V_G)$ of pristine graphene (PG) (dashed line) and CG (solid line) for the sweep up (red) and sweep down (black) branch at $T = 300$ K ($I = 1\mu$A). Four data points (1-2-3-4) are marked sequentially on the $R(V_G)$ curve. (b) Temporal response of R for CG ($T = 300$ K). Blue lines are fits to the data by an exponential curve with decay time τ_d and rise time τ_r. Measurements were conducted at $V_G = 0$ V following a sweep down (black curve) or sweep up (red curve) of V_G. Data in parts (a) and (b) are for the device shown in Figure 1a. (c) Schematic of the ferroelectric polarization in CIPS induced by a positive (left) or negative (right) V_G applied to the Si-gate electrode. The induced polarization **P** is parallel to the external electric field **E**. (d) Schematic of the charge transfer mechanism at the CIPS/graphene interface mediated by traps in the CIPS layer under a positive (left) or negative (right) V_G.

A non-volatile resistance switching and memristive effects can arise from a FE polarization in CIPS. For example, as sketched in Figure 2c, a positive gate voltage ($V_G > 0$ V) on the Si-gate electrode can induce a FE polarization in the CIPS layer that points upward, thus modulating the carrier density in the graphene layer. An opposite FE polarization should occur instead for $V_G < 0$ V (Figure 2c, right). However, our R (V_G) transfer curves do not indicate a well-defined switching gate voltage. Such observation is not consistent with an electric-field induced ferroelectric polarization reversal. As shown in Figure 3a, the amplitude of the hysteresis, as measured by ΔV_{NP}, increases monotonously with increasing the sweep voltage range. Also, the amplitude of the hysteresis decreases as the sweep rate increases (Fig. 3b). This

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contrasts with a ferroelectric polarization induced hysteresis as the dynamics of polarization reversal is much faster than the time scale considered in our study. Thus, the measured hysteresis should not display any dependence on the sweep rate if it were due to a ferroelectric polarization reversal. In general, an hysteresis due to a FE polarization should produce a shift of the Dirac point in the direction of the sweep [45], *i.e.* the neutrality point V_{NP} should shift to higher voltages when V_G is swept from negative to positive values compared to when V_G is swept from positive to negative values. This contrasts with the measured shifts in our devices (Figure 2a and 3). On the other hand, memristive effects and resistance switching can originate from other mechanisms, including electronic and/or ionic conduction in the FE layer. The ionization of dopants and/or a slow motion of ions within CIPS can be triggered by a large applied electric field and/or at high temperatures [25]. These can affect the conductivity of graphene through a charge transfer at the CIPS/graphene interface, as sketched for different V_G in Figure 2d. We now discuss and provide further investigations and analysis of these processes. In particular, we use a capacitance model of these hybrid FETs to account for the measured data.

2.2 Charge transfer at the CIPS/graphene interface

To account for a hysteresis in R (V_G) due to a charge transfer at the CIPS/graphene interface, we consider a classical capacitance model: a gate voltage increment ΔV_G generates an incremental increase in the charge ΔQ in the CIPS/graphene heterostructure, which we describe as $\Delta Q = C\,\Delta V_G$, where ΔQ is the sum of free charge carriers in the graphene layer (ΔQ_g) and charges bound onto localized states of CIPS (ΔQ_{CIPS}), and C is the capacitance of the SiO_2 layer. Here, we assume that the charge ΔQ redistributes between the graphene (Q_g) and the CIPS (Q_{CIPS}) layers with an effective time constant τ (ref. 58, Supplementary Information S3). The model takes into account the experimental sweep rate $\Delta V_G/\Delta t$, which is

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calculated by dividing the gate voltage sweep interval ΔV_G by the total measurement time interval Δt. Thus, the reading and waiting time at each point are taken into account.

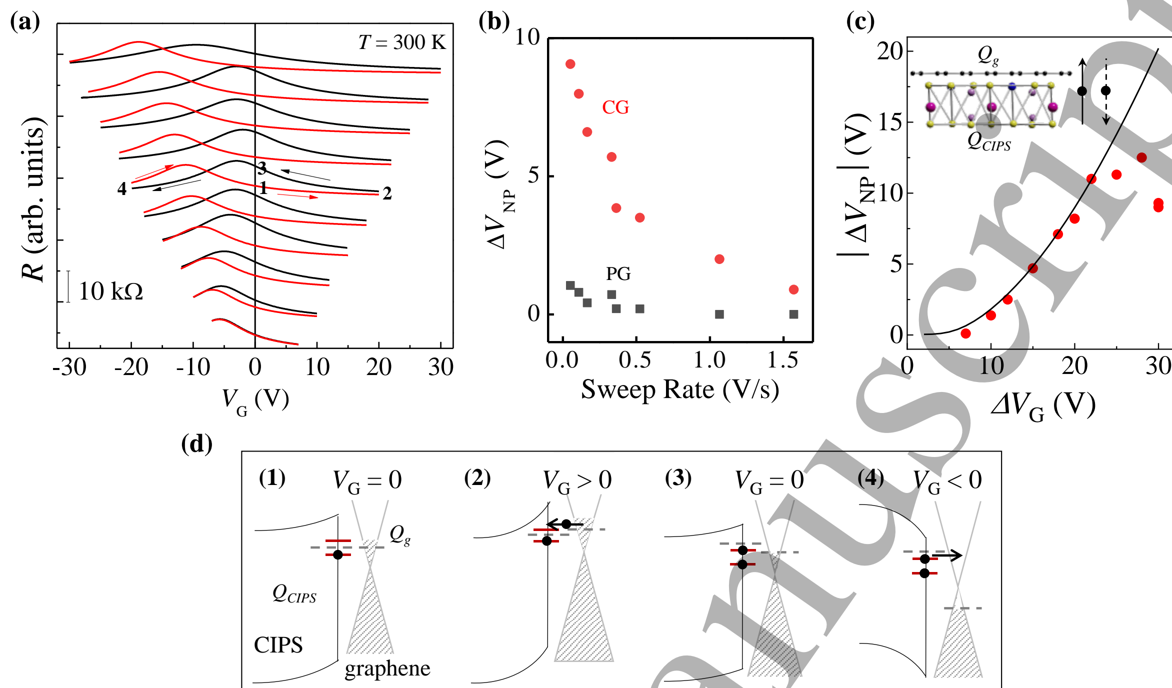

Figure 3: Transfer curves of CIPS/graphene (CG) for different ranges/rates of gate voltage V_G sweeps. (a) Transfer curves R (V_G) for CG at $T = 300$ K ($I = 0.3$ μA). The sweep up/down branches are shown in red and black, respectively. Curves are displaced along the vertical axis for clarity. Since PG and CG are measured using the same pair of terminals, to derive the $R(V_G)$ curve for CG, we have removed the contribution of PG from the measured transfer curve (see Figure S4 of the Supplementary Information). (b) The dependence of the amplitude of ΔV_{NP} on the sweep rate, with maximum V_G of 15 V. (c) Measured (red dots) and calculated (black line) amplitude of the hysteresis (ΔV_{NP}) versus the sweep voltage range ΔV_G. Inset: Schematic of the charge transfer process across the CIPS/graphene interface. (d) Band bending for CG. The electron affinity of graphene and CIPS is $\chi_{Gr} = 4.5$ eV and $\chi_{CIPS} = 3.7$ eV, respectively [20]. At $V_G = 0$ V, equilibrium is achieved by transfer of electrons between CIPS and graphene, inducing a depletion layer and an upward bend of the CIPS conduction band near its interface with graphene. Black dots correspond to trap charges and red lines illustrate the energy level of the traps. Different band alignments and charge transfers correspond to values of V_G marked as 1-2-3-4 in panel (a).

As shown in Figure 3c, our numerical calculations reproduce the measured dependence of the amplitude of the hysteresis ΔV_{NP} on the sweep range ΔV_G for a value of $\tau = 380$ s, which is the only fitting parameter. This time constant is in line with the characteristic times for switching on/off the resistance in the CG FET (Figure 2b). As the charges that can be transferred at the CIPS/graphene interface decrease with decreasing V_G, at low voltages the hysteresis

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disappears (Figure 3a). Also, above a threshold voltage of V_G ~ 20 V, ΔV_{NP} starts to saturate, suggesting a saturation in the charges bound to CIPS due to a finite density of charge traps. The direction of the hysteresis can be explained referring to the diagrams in Figure 2d and 3d. In the first part of the sweep of V_G to positive gate voltages ($V_G > 0$ V), negatively charged defects are created in CIPS by capture of electrons from the graphene layer. During the reverse sweep with $V_G < 0$ V, due to the negative gate potential, holes drift toward the interface and neutralize the defects. In summary, the hysteresis is caused by trapping of charges in the CIPS layer. The gate voltage induces charges in the graphene layer, which then redistribute between graphene and CIPS. This time-dependent slow process causes a hysteresis in the transport characteristics that depends on the sweep rate and range of the gate voltage.

We examine further this charge transfer by considering the T-dependence of the R (V_G) curves. As shown in Figure 4a, at low temperatures ($T \leq 200$ K), the hysteresis and memristive effects are very weak. A comparison of the R (V_G) curves for CG and PG at $T < 200$ K reveals that CIPS acts to n-dope the graphene layer. Thus, over this range of temperatures, the charge transfer across the CIPS/graphene interface involves shallow donor-levels in CIPS with a fast temporal trapping/detrapping dynamics. However, as the temperature increases above $T = 200$ K, the hysteresis in CG becomes more pronounced compared to pirstine graphene (Figure 4a and b) with a thermally activated behaviour described by $|\Delta V_{NP}| \approx \exp(-E_a/\kappa T)$ over the temperature range $T = 200 - 320$ K, where $E_a = 0.10 \pm 0.01$ eV is the activation energy (Figure 4c); a further increase of temperature above $T = 320$ K leads to a significant broadening of the transfer curves. The increase of the hysteresis with increasing T in CG is accompanied by a corresponding change of the electron density. For the sweep up of V_G, the electron density increases from $n \sim 4\times10^{11}$ cm^{-2} to $n \sim 1.3\times10^{12}$ cm^{-2} at $V_G = 0$ V (Figure 4d). The range of high temperatures ($T > 200$ K) in our experiments coincides with that required for the activation of the thermal motion of the Cu-ions, which leads to a progressive increase of disorder and ionic conductivity in CIPS for $T > 250$ K [31] and a paraelectric-ferroelectric transition at $T \sim 315$ K

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[28, 29]. The behaviour illustrated in Figure 3 and 4 was observed in all three of our CIPS/graphene FETs (see also Figure S4 in the Supplementary Information S2). Thus, the temporal dynamics of the resistance and hysteresis at large V_G and $T > 200$K suggest a slow charge transfer at the CIPS/graphene interface mediated by defects with deep localized states in the band gap of CIPS. Although model calculations predict an intrinsic, stable out-of-plane ferroelectricity in CIPS, charge transfer from/to defects across the CIPS/graphene interface can play a dominant role at $T > 200$ K. Since the range of temperatures at which the hysteresis occurs corresponds to the temperatures at which the Cu-ions are displaced from their lattice sites, we propose that the defects responsible for the hysteresis may form as a result of the thermally activated migration of the Cu-ions. Thus, the two phenomena, the thermal motion of the Cu-ions, which leads to a progressive increase of disorder, and the trap states due to the crystal disorder, could be linked.

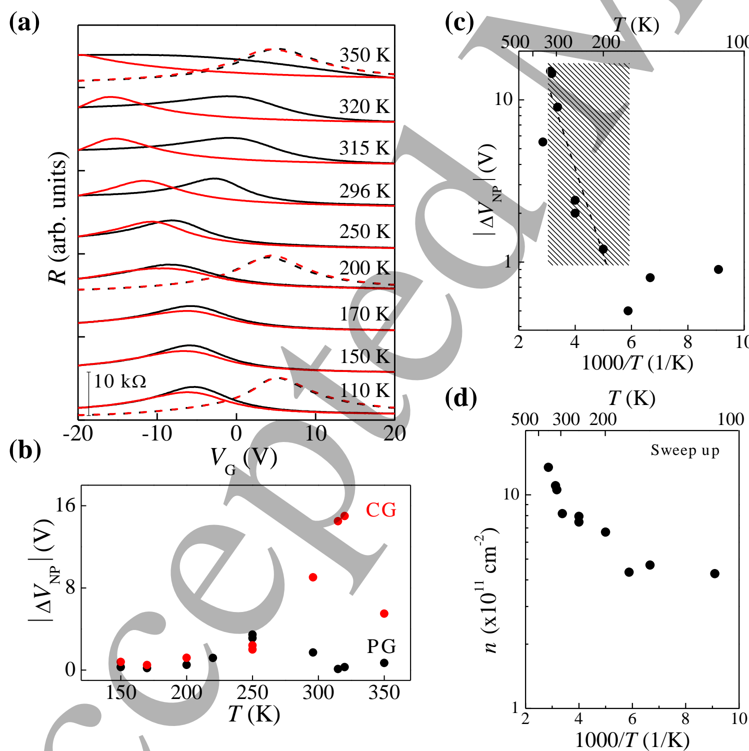

Figure 4: Transfer curves of CIPS/graphene (CG) at different temperatures. (a) Transfer curves $R(V_G)$ for CG at different temperatures T (I = 1 μA). The sweep up/down branches are shown in red and black, respectively. For clarity, curves are displaced along the vertical axis. $R(V_G)$ curves for pristine graphene (PG) are shown as dashed lines for T = 110 K, 200 K and 350 K. (b) Amplitude of the hysteresis $|\Delta V_{NP}|$ versus T, as derived from the data in part (a) for CG and PG. (c) Amplitude of the hysteresis $|\Delta V_{NP}|$ versus $1/T$, as derived from the data in part (a) for CG. The dashed line is an exponential fit to the data in the temperature range T = 200-320 K. (d) Carrier density, n, versus $1/T$ at $V_G = 0$, as derived from the data in part (a) for CG and sweep up branch of $R(V_G)$.

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We have investigated CIPS/graphene FETs based on CIPS layers with thickness ranging from about t = 50 to 135 nm. They all reveal hysteresis effects, although they tend to become more pronounced in thicker layers (for example, compare Figure S4d for t = 135 nm, Figure 3c for t = 52 nm and Figure 4a for t = 50 nm). This suggests that the charge transfer involves defects in the CIPS layer rather than defects at the CIPS/graphene interface. For thinner layers, the use of CIPS as an effective dielectric gate can be compromised by the loss of electrical insulation under a large applied electric field and/or temperature.

The electrical properties of thin CIPS layers were examined by considering tunnel junctions (TJ) based on a CIPS layer (t = 34 nm) embedded between two electrodes made of few layer graphene (FLG). Figure 5a shows the optical image and schematic of this TJ, whose current-voltage I-V curve was acquired over a range of V and T. As shown in Figure 5b, at T = 300 K, the I-V reveals a counter-clockwise loop: the amplitude of the current is larger when sweeping the voltage from high to low positive V (or from more negative to less negative V). The I-Vs are asymmetric with respect to the polarity of V, suggesting two nonequivalent interfaces. The increasing hysteresis with increasing the sweep range of V suggest that polarized charges at the CIPS/FLG interface can effectively lower or increase the potential barrier seen by electrons (Figure 5c) [40], causing a change of the electron transmission through the junction and resistance switching. In general, we cannot exclude a contribution of charge transfer in the TJ. The overall shape of the transport characteristics and hysteresis is influenced by both charge transfer and ferroelectric polarization effects. These two phenomena induce a different hysteresis, *i.e.* clockwise or counter-clockwise hysteresis, respectively. For example, as illustrated in Figure S5c-d in the Supplementary Information, the hysteresis behaviour tends to weaken with increasing T from 300K to 350K, suggesting that the ferroelectric switching is weakened by a thermally activated charge transfer. From the Arrhenius plots of the amplitude of the current versus 1/T, we extract an activation energy E_a = 0.3-0.5 eV for T > 200 K (inset of Figure 5b). As for the FET, this behaviour suggests a thermal excitation of charges from

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defects and/or ionic conductivity in CIPS. We estimate a break down electric field of about 5×10^7 V/m at T = 300 K, smaller than that of other commonly used dielectrics, such as nanometer-thick SiO_2 (~ 10^9 V /m) and hBN (~ 10^9 V/m) [63, 64]. The applied electric fields in this study (up to about 5×10^7 V/m) are higher or comparable to the reported coercive field of ~5×10^6 V/m (in bulk materials, ref. 65), ~14×10^7 V/m (in devices, ref. 20), and 1×10^7 V/m to 13×10^7 V/m (in PFM, ref. 18).

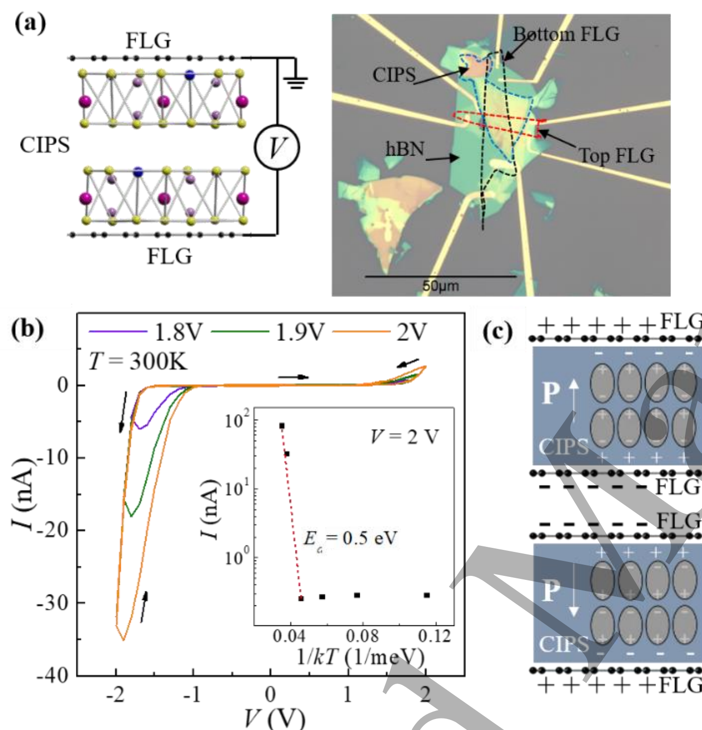

Figure 5: Tunnel junction based on CIPS and few layer graphene (FLG). (a) Left: Schematic of the FLG/CIPS/FLG junction. The bottom and top FLG comprise 7 and 3 graphene layers, respectively. The CIPS layer has thickness $t = 34$ nm. A voltage V is applied between the two FLG electrodes, generating a current I. Right: optical image of the device with the boundary of each flake traced by dashed lines. (b) I-V at T = 300 K, showing a counter-clowise hysteresis. Inset: Arrhenius plot of I versus $1/k_BT$ at $V = 2$ V, as derived from the I-V in Figure S5. (c) Schematic of surface polar charges and FE polarization in FLG/CIPS/FLG.

2.3 Photodoping effects

We exploit the semiconducting properties of CIPS and use light to probe further the charge transfer and hysteresis effects in the FETs. Figures 6a and b show the R (V_G) curves of CG at T = 100 K and 300 K under light illumination with laser light of wavelength $\lambda = 405$ nm and incident power P_i over a wide range from $P_i = 0$ (dark) to P_i ~ 2×10^{-8} W. At T = 100 K (Figure 6a) and low laser powers ($P_i < P_1 = 2\times10^{-13}$ W), the R (V_G) curves are not changed by light. In contrast, for $P_i > P_1$, the R (V_G) curves shift to negative gate voltages and the hysteresis becomes more pronounced. A distinct phenomenology is observed instead at room temperature.

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As shown in Figure 6b, at T = 300 K, increasing P_i above $P_2 = 1\times10^{-10}$ W leads to an upward shift of the R (V_G) curves, rather than the downward shift seen at T = 100 K. Thus, the photodoping effect in graphene changes from n-type (Figure 6a) to p-type (Figure 6b) with increasing temperature. At all temperatures, light enhances the hysteresis in R (V_G): The P_i-dependence of $|\Delta V_{NP}|$ at different T is illustrated in Figure 6c.

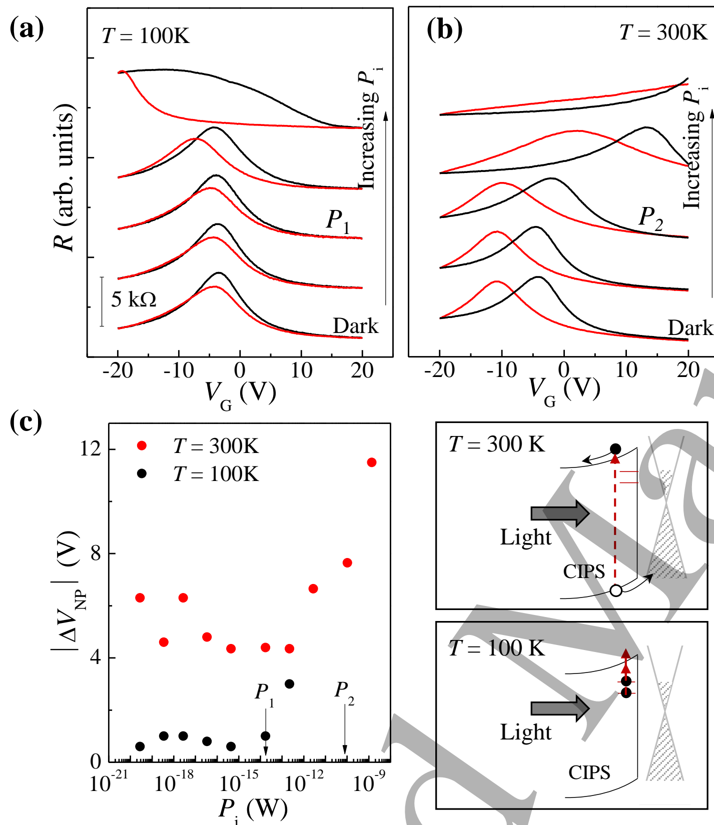

Figure 6: Transfer curves of CIPS/graphene (CG) under light illumination. Transfer curves $R(V_G)$ for CG for different laser powers P_i (λ = 405 nm) at (a) T = 100 K and (b) 300 K (I = 1 μA). Changes in $R(V_G)$ are observed for $P_i > P_1 \sim 2\times10^{-13}$ W (T = 100 K) and $P_i > P_2 \sim 1\times10^{-10}$ W (T = 300 K). The sweep up/down branches are shown in red and black, respectively. For clarity, curves are displaced along the vertical axis. (c) Amplitude of the hysteresis $|\Delta V_{NP}|$ extracted from the transfer curves versus P_i in parts (a-b). Inset: Schematic of the separation of photocreated carriers by the electric field in CG (top) and the ionization of traps by light (bottom).

The light-induced hysteresis and photodoping of graphene are activated above a critical laser power that depends on temperature. We propose that at low temperatures, donor-like states in CIPS and/or at the CIPS/graphene interface are ionized by light, acting effectively as a local positive gate for the graphene channel. The photo-ionization of defects increases the electron density in the graphene layer and reduce the carrier mobility due to enhanced carrier scattering by ionized impurities (bottom inset of Figure 6c). In contrast, at room temperature, photo-created holes are accelerated towards graphene by the electrostatic potential of the CIPS/graphene interface (top inset of Figure 6c). This potential arises from the ionization of defects in CIPS leading to an increasing charge transfer at the CIPS/graphene as the temperature

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increases. We note that the light-induced effects tend to be weaker at gate voltages far from the neutrality point of graphene as the change in carrier density due to the gate becomes stronger than the light-induced change. The hysteresis and slow dynamics of the resistance change under light illumination (Figure S6 in the Supplementary Information) are indicative of a light-activated slow redistribution of charges. This is a reversible process, suggesting a dynamical disorder tuneable by light. Previous studies have examined the absorption spectrum of CIPS, revealing an extended Urbach tail near the absorption edge due to localized states [59, 60]. Our photoluminescence (PL) studies reveal the existence of localized states in both bulk and nanometer-thick CIPS flakes. They have a room temperature PL emission centred at 1.9 eV, lower than the direct band gap energy of CIPS. The energy peak position of the PL emission is weakly affected by temperature, shifting by about 20 meV to high energy with decreasing T from 300 K to 10 K (Figure S2 in the Supporting Information S1).

3. Conclusion

In conclusion, we have shown that bringing CIPS into contact with a graphene layer triggers a range of complex phenomena. We have reported a large hysteresis effect in field effect transistors where the graphene layer acts as a channel and CIPS behaves as a charge trapping layer. The underlying mechanisms of conduction were examined over a range of temperatures and under light illumination to account for different resistive switching mechanisms. The measured effects indicate a slow (> 100 s) charge transfer between CIPS and graphene at temperatures $T > 200$ K. Charge transfer can occur in darkness and under light illumination. In particular, light induces a temperature-dependent photodoping effect in graphene that varies from n- to p-type with increasing temperature. The measured electrically and optically controlled memristive effects in these devices highlight the complexity of the graphene/CIPS heterostructure. Charge transfer mediated by defects in CIPS can influence the tunneling resistance of FTJs and the operation of other ferroelectric devices, such as FeFETs.

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The addition of an hBN barrier layer could prevent the charge transfer at the CIPS/graphene layer, facilitating the observation of the ferroelectric switching, as done in recent work with other 2D ferroelectrics [44]. Thus, engineering the interface of graphene with ferroelectrics should consider the contribution of both charge transfer and polarization effects for device optimization and a rich variety of new applications. Our experimental findings will stimulate further work, including the modelling of the graphene/CIPS interface (and other hybrid interfaces) beyond the current literature, which neglects the contribution of charge traps. The fully two-dimensional ferroelectric/graphene heterostructure represents an emergent platform that could drive exciting advances in modern electronics. Being a vdW crystal, CIPS can form an ideal interface with graphene and other vdW crystals. Also, unlike many ferroelectrics, CIPS is a semiconductor, well suited for modulation of electrical properties by light.

4. Experimental Section

Materials and device fabrication The $CuInP_2S_6$ (CIPS) crystal was purchased from HQ Graphene. To fabricate the CIPS/graphene Hall bars, graphene grown by chemical vapour deposition (CVD) was transferred on top of the exfoliated CIPS flake on a SiO_2/Si substrate (SiO_2 layer thickness of 300 nm) using a needle-assisted transfer process within a glove box at the Institute of Semiconductors in Beijing, China, as described in ref. [66]. The whole device was then spin coated with polymethylmethacrylate (PMMA) at 4000 rpm for 1 minute to define an etching mask to create a graphene Hall bar. Immediately after spin-coating, the substrate was transferred to a pre-heated hot plate at 150 ^{o}C for 3 mins. Electron beam lithography (EBL) with a Nanobeam nb5 EBL instrument at the Nanoscale and Microscale Research Centre (nmRC) in Nottingham was used to pattern the Hall bar. The graphene layer was shaped into a multi-terminal Hall bar by reactive ion etching (RIE) using Ar/O_2 plasma for 20 sec (working pressure 30 mTorr; RIE power 60 W; Ar flow rate = 80 sccm; O_2 flow rate = 20 sccm). The EBL patterned PMMA layer was utilized as an etching mask. The etching was done using a Corial 200IL RIE/ICP plasma etcher operated by a COSMA process control software. The area

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of CIPS that was exposed to the etching is not the area of the flake directly underneath the graphene Hall bar. Thus, we exclude any significant influence of the etching process on the measured effects. After this step, the device was developed using a solution of isopropyl alcohol and methyl isobutyl ketone (3:1) for 3 mins. Finally, contact pads based on titanium-gold (Ti/Au) were deposited using a thermal evaporator before doing lift-off in acetone for 2 hrs.

The FLG/CIPS/FLG heterostructures and devices were fabricated at the National Graphene Institute (University of Manchester). The fabrication method is as follows. First, a CIPS flake was exfoliated and transferred onto a a 290 nm-thick SiO_2/Si substrate coated with a polypropylene carbonate. Then, a thin hBN layer (~30 nm) on a PMMA membrane was used to pick up a FLG flake. Subsequently, the FLG/hBN/PMMA membrane was used to pick up the CIPS flake. The final stack of CIPS/FLG/hBN on the PMMA membrane was transferred onto a FLG/hBN/SiO_2/Si substrate. Thus, the FLG/CIPS/FLG stack is encapsulated within thin hBN layers. For electrical characterization of the tunnelling devices, Cr/Au edge contacts were made on the top and bottom FLGs using EBL, followed by hBN etching, metal deposition and a lift-off process. The hBN flake was etched by reactive ion etching using CHF_3 and oxygen. Four contacts were made on the FLG sheets. For the heterostructure assembly, the top and bottom FLGs were chosen to extend beyond the CIPS layer to avoid any effect of the processing (especially the top hBN etching and subsequent lift-off process) on the properties of CIPS.

Optical, electrical and microscopy studies The surface topography of the flakes was acquired by atomic force microscopy (MFP3D in Nottingham and Dimension FastScan in Manchester) in non-contact mode under ambient conditions. The Raman and photoluminescence (PL) spectra for CIPS were measured using a confocal microscope from Horiba Scientific equipped with 150 (PL) and 1200 (Raman) grooves/mm gratings and a range of objectives (10x, 50x, 100x) to focus the laser beam onto the sample. The samples were mounted on a linear positioning stage and were excited by a frequency-doubled Nd:YVO4 laser (λ = 532 nm). The Raman and PL signals were detected using a CCD (Charge Coupled Device). Transport

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measurements in the dark and under light illumination were conducted in vacuum (2×10^{-6} mbar) using Keithley-2400 source-meters and Keithley-2010 multi-meters. A temperature controller from Lakeshore Cryotronics was used to control and probe the temperature. A laser light source ($\lambda = 405$ nm) from Thor Labs was used to study the electrical transport under light illumination. The position of the laser spot was adjusted on the device and measurements were taken at different powers.

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Supporting Information

Supporting Information is available online or from the authors.

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Conflict of interest

The authors declare no conflicts of interest.

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